ENGINEERING NOTEBOOK

ATARI™

ATARI®

VISITOR

NAME JOSEPH DECUIR

DATE 27 MAY 81

A Warner Communications Company

ENGINEERING NOTEBOOK

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3. Clarity is essential but precision drawings are not required; therefore, free-hand sketches are acceptable.

Book No. 76078 ***Assigned to*** Joe Decuir

ATARI **ENGINEERING LOG SHEET** 1

GAME OR PROJECT
COLLEEN / ANTIC.

BEGINNING THIS 2ND ATARI LOGO ENGINEERING NOTEBOOK. 6 JANUARY 1978

THE NEXT YEAR IS FOCUSED ON THE DESIGN OF THE ANTIC CHIP,
AT THIS POINT, MOST OF THE FUNCTIONS OF ANTIC HAVE BEEN SPECIFIED, AND A BLOCK DIAGRAM CREATED. DESIGN REVIEWS OF THE 3 CHIPS AND SYSTEM WERE HELD ON 21 DEC 77

JAY ~~MINNER~~ IS THE OVERALL CHIEF ENGINEER.
I WILL ASSUME RESPONSIBILITY FOR ANTIC, AND GET HELP IN LOGIC DESIGN FROM FRANCOIS MICHEL.
GEORGE McLOED WILL FOCUS ON THE 2ND GENERATION TIA, WHICH HANDLES 8 MOVING OBJECTS, COLLISIONS, AND VIDEO GENERATION.
DOUG NEUBAUER WILL FOCUS ON THE POKEY, WHICH HANDLES: POT SCAN, KEYBOARD SCAN, SERIAL PORT, AND AUDIO.
SCOTT SHIRMAN WILL FOCUS ON THE ~~REST~~ WHOLE DIGITAL SYSTEM, INCLUDING THE MPU, 3 CUSTOM LSIS, PIA, RAMS, ROMS BUFFERS, DECODING, INTERCONNECT. ETC...
AL MILLER WILL JOIN US AS APPLICATIONS PROGRAMMER AND ALL AROUND HARDWARE/SOFTWARE TYPE. - MAYBE RAM SELECTION, AND ~~DESIGN~~ DETAILED DESIGN OF SERIAL ~~PORT~~, COMMUNICATIONS PROTOCOL
HOWARD BORNSTEIN IS THE FIRST MAN TO LOOK AT THE SYSTEM MONITOR/RESIDENT FIRMWARE.

WRITER ~~EC~~ DECKER	DATE 6 JAN 78	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
ANTIC.

SUMMARY TO DATE.

ANTIC IS A STATIC GRAPHICS GENERATOR, PROGRAMMED DMA ~~BUS~~ CHANNEL FROM MEMORY TO THE SCREEN.

FUNCTIONAL BLOCKS INCLUDE:
- CLOCK GENERATOR
- HSYNC ~~AND VSYNC TIMER AND~~
- VSYNC
- ADDRESS DECODE
- DMA INSTRUCTION REGISTER
- DMA INSTRUCTION DECODE LOGIC
- INTERRUPT LOGIC
- ADDRESS GENERATORS: DISPLAY LIST
  - OBJECTS
  - ~~MEMORY SCAN~~
  - CHARACTERS
  - REFRESH
- SCROLLING LOGIC.
- DISPLAY BUFFER RAM 48x8
- RAM ADDRESS CONTROL
- GRAPHICS ~~SERIAL/PARALLEL~~ SR.
- VIDEO ENCODING PLA
- DRIVERS TO TIA
- DATA BUS TRANCEIVERS.
- ~~DMA~~ ~~REGISTER~~ BUS CONTROL LOGIC

WRITER	DECKER	DATE	6/84.	WITNESS		DATE	

GAME OR PROJECT: COLLEEN/CANDY

DEFINITION MEETING.

AL, JOHN ELLIS
JAY, JOHN ULRICH,
JOE, HOWARD
WADE, NILES, SCOTT

NILES THINKS WE CAN USE 4K MUX DYNAMICS. 4027

4K 18 PIN ~~NON~~ MUX DYNAMIC (4050) NEEDS 12V CLOCK
4K 22 PIN NON MUX DYNAMIC (2107) INVERTED DATA I/O.
4K 18 PIN STATIC 4044 - EXPENSIVE, EATS POWER

TOM WANTS DECISION MADE SO WE CAN DICKER PRICES

~~COLEEN~~ ADD 'CHEAP' AUDIO CASSETTE INTERFACE TO CANDY AND COLLEEN.
INCLUDING MOTOR ON/OFF

	COLLEEN:	CANDY:
DIFFERENCES.	CHIP SET	CHIP SET
	4K RAM	4K RAM
→	2 CARTRIDGES	1 CARTRIDGE
	3 PANEL SWITCHES	3 PANEL SWITCHES
→	BUILT IN KYBD	PLUG IN KYBD ON PORT 3,4
	4 JOYSTICK PORTS	4 JOYSTICK PORTS,
	AUDIO CASSETTE I/O	AUDIO CASSETTE I/O.
→	SERIAL PORT	NO SERIAL PORT.
→	~~BUS~~ EXPANSION	NO BUS EXPANSION.

WRITER ~~JOE~~ JOE DECUIR | DATE 1/MAY | WITNESS | DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

MEETING W/ GLASS VALLEY CASSETTES/DISKS

LARRY FULMONTS
STEVE MAYER
GENE WISE
TOM MILNER

JOHN ELLIS
WADE
NILES
DAVE ESTES
RICH PAP.

JAY SCOTT
JOE HOWARD

JOHN IS LOOKING FOR
CHEAP AUDIO CASSETTE, PAUSE CONTROL
STEREO? FOR DOBBERT
< 20 IN 200K

PRESENTATION ABOUT PROBLEMS
ON CASSETTES BY LARRY FULMONTS

2 TRACK VS 4 TRACK HEAD PROBLEMS
→ TRACK WIDTH,
GAP WIDTH VS FREQUENCY RESPONSE

DISCUSSION BETWEEN
FREQUENCY MULTIPLEXING DIGITAL AND ANALOG —
OR SEPERATE TRACKS FOR
DIGITAL AND AUDIO

USE A SMART CASSETTE LATER.

NILES AUDIO CASSETTE IS AN FM TYPE
RECEIVER/XMITTER, CAN TOLERATE
TO -50db ATTENUATION AND STILL RECOVER DATA

CAN THEY USE THE AUDIO CASSETTE
I/O AS A SIMPLE MODEM, TOO?

WRITER JOE DECUIR	DATE 13 JAN	WITNESS	DATE

GAME OR PROJECT
SAME AS p4.

fully asleep

HOW DO WE DESIGN THE SYSTEM TO PROTECT OUR SOFTWARE?

CHEAP BUILT IN AUDIO 1 PROBLEM MANUAL CONTROL

SMART SERIAL PORT CASSETTE 2ND PROBLEM AUTOMATIC CONTROL.

LONG TERM – FLOPPIES AND PRINTERS,

SLOW FLOPPY V1.5

35 RPM,
MECHANICAL HEAD MOVING INDEX MECHANISM.
18 TRACKS 270° PULSE OR COM
(THEY'D LIKE 10) 90° FALLOFF
CASSETTE HEAD
#13 FOR PARTS. BAUD RATE ~1.5 to 2x CASSETTE
4-6 KBAUD.

40- 80 mil track SPACING

WHAT IS HEAD SPACING TOLERANCE.

MUCH THINKS THAT MAY PERIPHERALS SHOULD
BE TWO TIERED SID OUT EARLY
OUR DESIGN LATER
CASSETTES, PRINTERS & DISKS.

WRITER	JOE DECUIR	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
COLLEEN.

RON'S PRINTER.

SCAN MECHANISM 50
+ VICTOR PRINT HEAD. 35
OTHER PARTS ?

ATARI **ENGINEERING LOG SHEET** 7

GAME OR PROJECT
COLLEEN/CANDY MEETING 31JAN.

CANDY. ALL GAME PLAYER CARTRIDGES COMPATIBLE W/ COLLEEN.

JOHN UNGER
AL, WADE, JOHN ELLIS, JAY MINER, SCOTT SHERMAN
JOHN HAYASHI, DAVE ESTES, HOWARD BERNSTEIN,
NILES STROHL, LARRY KUBBINS, JOE DECUIR, ?

- POINTS DISCUSSED: (1) → CANDY KEYBOARD ON SEPERATE CONNECTOR OR COMMON CONNECTOR

(2) → CANDY PERIPHERALS
CONSOLES IS YES
CHEAP KEYBOARD
CHEAP CASSETTE
MODEM? → ACOUSTIC COUPLER.

↳ POKEY - 2 TIMERS RUNNING BAUD RATE
2 TIMERS GENERATING MODEM TONES

CASSETTE DEMODULATOR IN MAINFRAME.

(3) → HOW MANY CHIPS CAN GO INTO CANDY CARTRIDGES.
CANDY, COLLEEN CARTRIDGES MIGHT BE DIFFERENT SIZES
↳ 24 PIN PACKAGES. (32K ROMS)

WRITER	DATE	WITNESS	DATE
JOE DECUIR	~~31JAN~~ 78		

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
COLLEEN ETC.

ELIZABETH

(4) BUILT IN CRT COLOR MONITOR

223 → COLOR MONITOR 150

$273 COST FOR ELIZABETH.

COLLEEN $127

SEPERATE CABINET FOR MONITOR. 12"-13" SLOT MASK,

(5) WHAT HAPPENS TO BUS EXPANSION BOX.

MAY BRING BUS TO KNOCK OUT CONNECTOR.

SLOW FLOPPIES - ONLY ON SERIAL PORT.

(6) NO BLACK & WHITE SWITCH.

(7) PUT ALL CONNECTORS TOGETHER?!

(8) POSSIBLE FUTURE REMOTE CONTROLLER.

WRITER JOE DECUIR	DATE 3/30/84	WITNESS	DATE

GAME OR PROJECT
COMPUTER, ETC.

(9) CONNECTORS & PLAYER CONTROLS
? AUDIO OUT
AC.
? VIDEO OUT NTSC. PAL
RF OUT.

(10) KEYBOARD - CURSOR CONTROL.
KEYBOARD UP TO $19!!

(11) DESIGNED [redacted] 4Y POT

(12) LIGHT PEN. / STILL MAYBE

(13) ROM SLOT CASSETTE
SLOT FLOPPY
PRINTER
MODEM?
AC CONTROLLER ????
ACOUSTIC

(14) SERIAL PORT.

(15) PRINTER

WRITER DECUIR | DATE 5 JAN 78 | WITNESS | DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
Colleen — NEW 6500 PROCESSOR.

6502 REG.
MIKE ASSAR (RON SPRINGER PROJECT LEADER)
WILL MATHYS
JAY MINER, AL MILLER, JOE DECUIR

1. SATISFY ATARI
2. SUPER MACHINE FOR WHOLE COMPUTER
3. UPGRADE, DEFINE 6502 SOCKETS
   180 MIL RANGE.
   (currently 145 x 155)

POINTS

WE COULD USE UPPER BYTE OF STACK AS STACK PAGE POINTER.

(1) — PROBABLY JUST MAKE IT MULTIPLE CYCLE INCREMENT ACROSS PAGE BOUNDRY.

(2) MORE ON Z REGISTER

PREFER LOAD Z IMMEDIATE
PUSH Z PULL Z.
MAYBE TZA, TAZ.

LZP, SZP (LOAD AND STORE ZERO PAGE)

WHY HAVE THIS?

WRITER	DECUIR	DATE	1/13/78	WITNESS		DATE	

GAME OR PROJECT

NEW PROCESSER

	A	X	Y	
00	8	8	8	✓
01	16	8	8	
10	16	8	16	
11	8	16	16	✓
100	8	8	16	
101				
110				
111	8	16	8	

STATES SUGGESTED COMPROMISE.

FITS IN CURRENT STATUS REGISTER.

? SHOULD WE HAVE 3 16 BIT REGISTERS

HOW ABOUT 3 BIT STATUS REGISTER
LOAD IMMEDIATE, PH, PL.

STATE COUNTER DONE W/SR!

ADD 3 REGISTERS INSTEAD OF TWO.

AND 3 BIT ATTACH/DETACH REGISTER.

	N	V	F	B	D	I	Z	C

A	ACH	ACL
X	XH	XL
Y	YH	YL
S	SPH	SPL
PC	PCH	PCL
Z	Z	

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ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
Convert. - New Mpu.

ADD REGISTER SWAPS, ?

ACL → XH, YH } 4
XH, YH → ACL

ACL ⇄ ACH. } 1

~~ACL ⇄ ACH~~

OR

~~ACH → ACL~~
XH → ACL
YH → ACL

~~ACL~~
AL
AL

QUESTIONABLE XH ⇄ XL
YH ⇄ YL

2 OPCODES { DXB, ~~DXBI~~ } DECREMENT XH AND BRANCH
DYB " YH AND BRANCH

2 { MAYBE LXHI
LXYI

WRITER	DECKER	DATE FEB	WITNESS	DATE

GAME OR PROJECT
NEW ANAL.

AUTO INCREMENT, DECREMENT MAY BE
REAL TROUBLE.

BECAUSE CROSSING PAGE
BOUNDRIES MAY CAUSE
FATAL PROBLEMS WITHIN
THE OVERLAPPED CYCLES.
AND ADDS EXTRA BUS

ANX, ANY - IMPLIES SIGN EXTENSION,
OF AN 8 BIT TWO'S
COMPLEMENT QUANTITY.

DISCUSSIONS ALL DAY 2 FEB 78

DEFINED PER FILE
OF CODE MAP - 1ST PASS.

AGENDA FOR 3 FEB.

1. PRECISE DEFINITION OF ADDRESSING MODES
2. INTERRUPT STRUCTURE
3. PINOUT
4. PROJECT SCHEDULE
5. DOCUMENTATION, HARDWARE AND PROGRAMMING
6. 6509 EMULATOR
7. CROSS ASSEMBLER.

WRITER	DECUIR	DATE	FEB	WITNESS		DATE	

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
6509

IMMEDIATE LOADS

ADC, ADD, SUB, SBC
AND, ORA, EOR, CMP.

LDA
LDX
LDY

2 BYTE OR 3 BYTE
DEPENDING ON
ATTACHMENTS
OF A, X, Y
TO ASSEMBLER.

ZERO PAGE (Z:B2) → REG

INSTRUCTION
ALWAYS 2 BYTES

OR (Z:B2) → { 16 BIT REG. AL, XL, YL
(Z:B2+1) → { AH, XH, YL

#1 STD. (Z:B2+XL) → ZP,X, (ZP,Y)

#2 A ATTACHED (Z:B2+XL) → { 16 BIT REG.
(Z:B2+XL+1) → {

#3 X ATTACHED. (Z:B2+XL) → { 16 BIT REG.
(Z:B2+XL+1) → {

TAKES NEW CYCLE TO ADD CARRY

XH IGNORED, Z ALWAYS USED.

WRITER DECKER	DATE 3 FEB	WITNESS	DATE

GAME OR PROJECT
6509

ABSOLUTE

3 BYTE

B3, B2 → DATA REGISTER 8 BITS.

B3-B2 → {DATA}
B3+B2 → {DATA} REGISTER 16 BITS.

ABSOLUTE INDEXED, AB, X. AB, Y

~~B3+B~~

X STRAIT 0+B3+C : B2+XL

X CARRY or B3+XH+C : B2+XL

(ZP, X) (Z: B2+X) → ADL
(Z: B2+X+1) → ADH } → OPERAND.

2 BYTE

(AB, X) ~~X ATTACHED.~~

ALWAYS TWO BYTES

(ZP), Y

(Z: B2) → ADL +YL
(Z: B2+1) → ADH +YH +C } → OPERAND.

2 BYTE

(ZP)

(Z: B2) → ADL
(Z: B2+1) → ADH } → OPERAND.

2 BYTE

WRITER DEAN DATE ~~SEPB~~ WITNESS DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
6509

ASLA, ROR, ROL, ETC.

ALL ACC OPERATIONS ARE
SINGLE OR DOUBLE LENGHT.

NOTE DO WE NEED DOUBLE

LENGHTH ~~SHIFT~~ ~~COUNT~~
INCREMENT, DECREMENT ABSOLUTE.

CONVERTIONS

IF 8 INTO 16.

UPPER BYTE BECOMES ϕ

TO DO SINGLE CYCLE TRANSFER —
2ND - HIGH ORDER BUS.

WRITER	DATE	WITNESS	DATE

GAME OR PROJECT 6509

SOE (I) REQUEST

AN INTERRUPT ACKNOWLEDGE.

$\phi 1$ CLOCKED SIGNAL. 2 CYCLES

LONG - COINCIDENT WITH VECTOR FETCH.

$\overline{RES}$

$\overline{NMI}$

$\overline{IRQ}$

IRQ ACKNOWLEDGE = 

BRK

BRE

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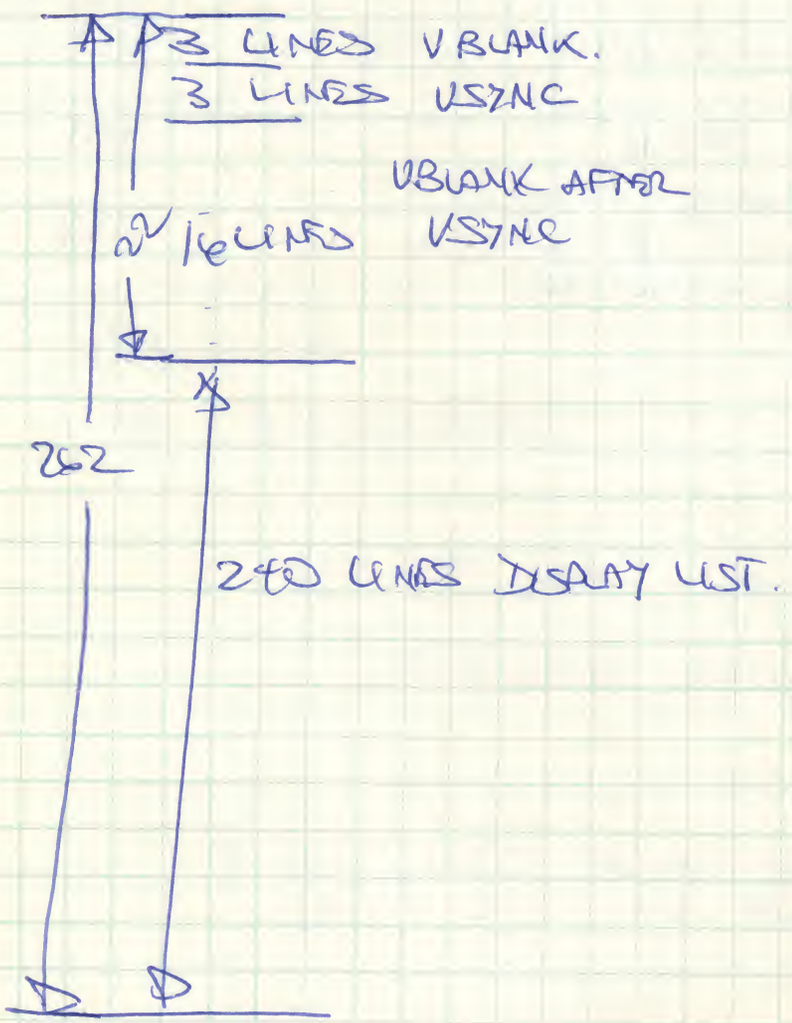
GAME OR PROJECT
ANTIC

DECISION TO DATE.

NO PARTICULAR REASON



WRITER	DATE	WITNESS	DATE

GAME OR PROJECT
ANTIC.

SUMMARY REVISIONS.
THIS WEEK.

PINOUTS = (2) VSS, VCC
(3) 3.58 IN. ϕ_0 OUT, ϕ_2 IN
(5) $\overline{RES}$, $\overline{NMI}$, $\overline{HALT}$, REF, R/$\overline{W}$
(8) DB0 - DB7
(16) AB0 - AB15
(4) AV0, AV1, AV2, CSYN
(1) $\overline{LP}$

39 PINS.

LOGIC AND SUCH.

DISCONNECT VSYNC COUNTER FROM REFRESH FUNCTION — AND HAVE SEPARATE REFRESH COUNTER.

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GAME OR PROJECT
ANTIC

VERTICAL CONTROL.

LAST LINE = STANDARD END
OR ΔCTR = IR6,5,4
OR ΔCTR = VSCROLL

FIRST LINE = LAST LINE +1 DELAY.

$\overline{NMI}$ = LAST LINE AND IR7 AND MODE NMI ENAB

~~CLEAR VSCROLL FLA~~
CLEAR START VSCROLL FLAG = LAST LINE • RES HSYNC

CLEAR END VSCROLL FLAG = FIRST LINE • RES HSYNC.

I_1 = I_1 WINDOW AND FIRST LINE

I_2, I_3 = CONDITIONAL DELAYS FROM I_1 • IR5

LOADΔ = 1ST LINE AND I_2 TIME

RAM WRITE = 1ST LINE • STROBE FROM 6 PLA

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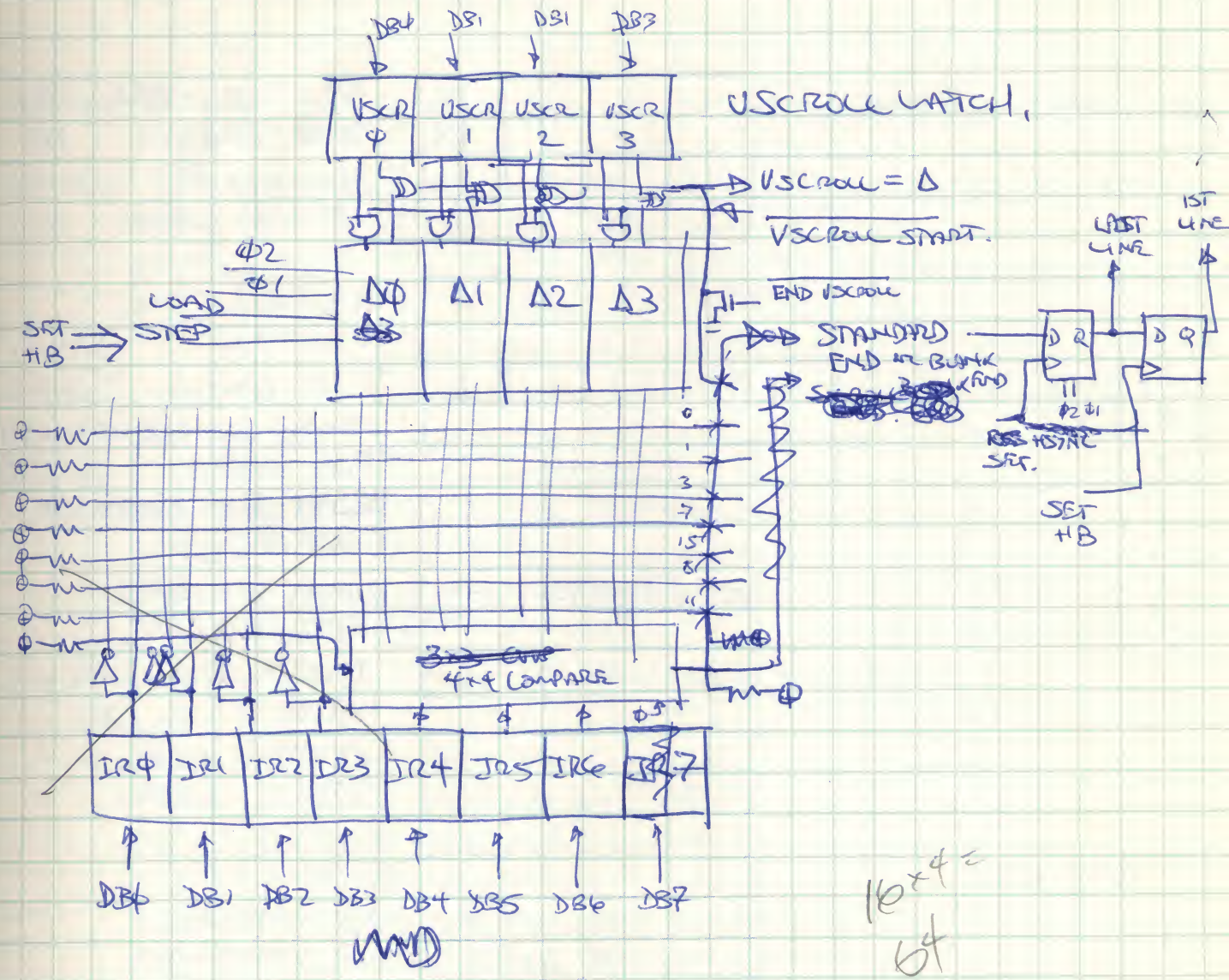
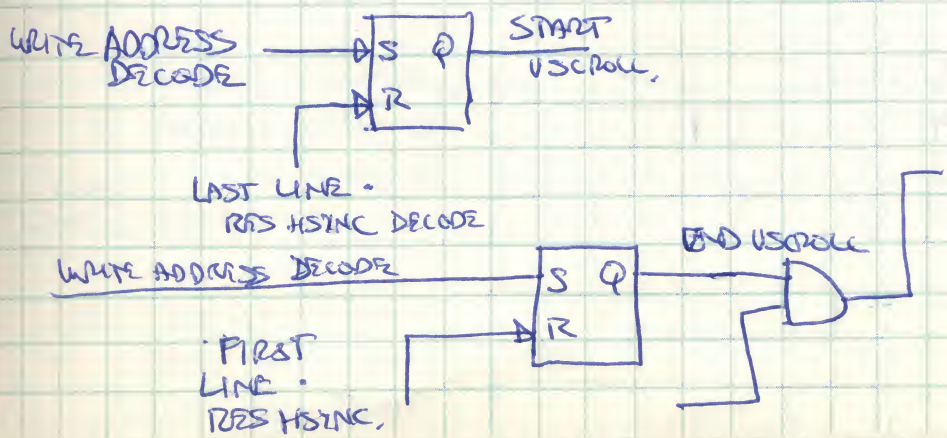
GAME OR PROJECT
ANTIC

VERTICAL CONTROL LOGIC



16 x 4 = 64



WRITER	DECUIR	DATE 7-16-78	WITNESS	DATE

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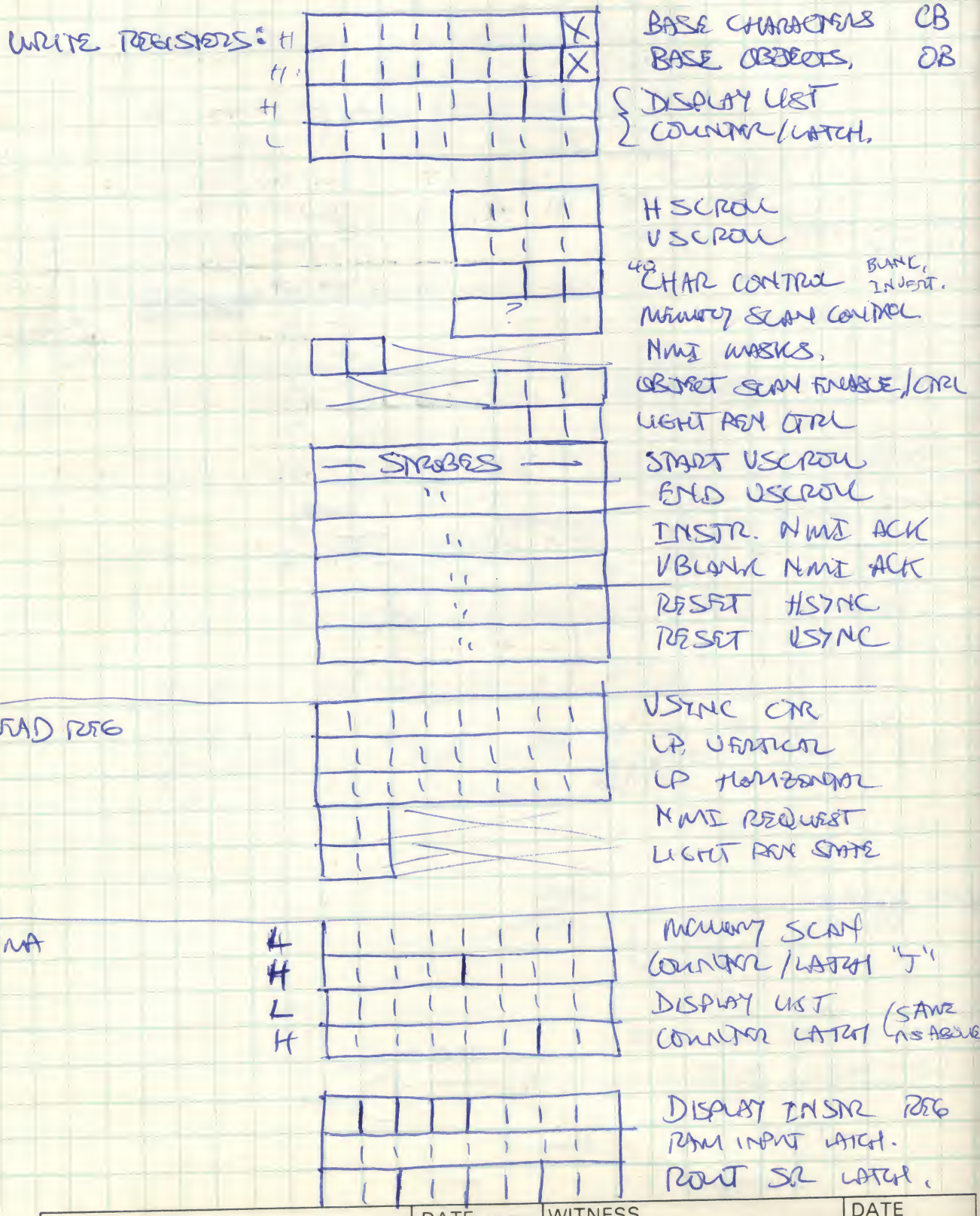
GAME OR PROJECT
ANTIC

REVISED REGISTER FILE



WRITER	DATE	WITNESS	DATE
DECKER	7/26/78		

GAME OR PROJECT
ANTIC

REVISED. ADDRESS TABLES.

	A15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Aϕ
REFRESH. *	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	RF6	RF5	RF4	RF3	RF2	RF1	RFϕ
OBJECTS/ MISSLS. 128 (OB) SCAN (MB)	OB_7	OB_6	OB_5	OB_4	OB_3	OB_2	$\frac{OB_1}{OB_1}$	$\overline{H1}$	Hϕ	OC_6	OC_5	OC_4	OC_3	OC_2	OC_1	$OC_ϕ$
256 (OB) SCAN (MB)	OB_7	OB_6	OB_5	OB_4	OB_3	$\frac{OB_2}{OB_2}$	$\overline{H1}$	Hϕ	OC_7	OC_6	OC_5	OC_4	OC_3	OC_2	OC_1	$OC_ϕ$
MEMORY SCAN	MSL 15	MSL 14	MSL 13	MSL 12	MSC 11	MSC 10	MSC 9	MSC 8	MSC 7	MSC 6	MSC 5	MSC 4	MSC 3	MSC 2	MSC 1	MSC ϕ
CHARACTER ADDRESSES 20/5	CB_7	CB_6	CB_5	CB_4	CB_3	CB_2	CB_1	CH5	CH4	CH3	CH2	CH1	CHϕ	Δ2 / Δ3	Δ1 / Δ2	Δϕ / Δ1
10/2	CB_7	CB_6	CB_5	CB_4	CB_3	CB_2	CH6	CH5	CH4	CH3	CH2	CH1	CHϕ	Δ2	Δ1	Δϕ
20/4	CB_7	CB_6	CB_5	CB_4	CB_3	CH7	CH6	CH5	CH4	CH3	CH2	CH1	R/L (65) / Δ3	Δ2	Δ1	Δϕ / Δ1
DISPLAY LIST	DL 15	DL 14	DL 13	DL 12	DL 11	DLC 10	DLC 9	DLC 8	DLC 7	DLC 6	DLC 5	DLC 4	DLC 3	DLC 2	DLC 1	DLC Φ

RF = REFRESH COUNTER 7 BITS.
OB = OBJECT BASE LATCH 7 BITS.
OC = OBJECT COUNTER 8 BITS.
MSL = MEMORYSCAN LATCH 4 BITS
MSC = MEMORY SCAN COUNTER 12 BITS
CB = CHARACTER BASE LATCH 7 BITS
CH = RAL = RAM ADDRESS LATCH = CHARACTER LATCH 8 BITS.
Δ = INSTRUCTION VERTICAL COUNTER BLOCK.
DLC = DISPLAY LIST COUNTER (10 BITS)
DL = DISPLAY LIST LATCH (6 BITS)

WRITER	DATE	WITNESS	DATE
DECKER	2/28/78		

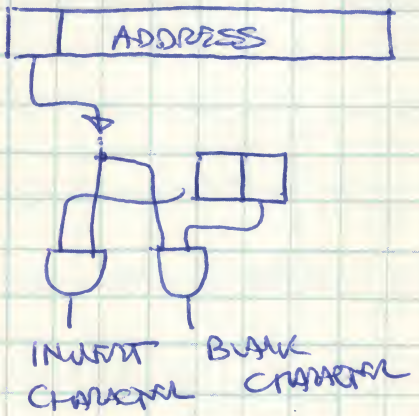
ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
ANTIC.

LONG CHAT W/ PROGRAMMERS YESTERDAY

1) PRESENT CURRENT INSTRUCTION SYNTAX.

2) CHANGE CHARACTER FORMAT IN 40 CHARACTER TO:



3) IDEA FROM HOWARD.

USE CHO BIT IN 2/4

TO INVERT 1 of 2 COLOR BITS

WRITER DAN | DATE | WITNESS | DATE

GAME OR PROJECT
ANTIC/CTIA CODES

FROM DISCUSSION W/ GEORGE ON THURSDAY 9 FEB

3 CODES TRANSMITTED TO CTIA AT 3.58 MHz RATE.

AN2, 1, 0

~~000~~ COMPOSITE BLANK / CLEAR 7MHz MODE
011

001 VSYNC / TEST (000 → 001)

010 CBLANK / SET ~~[illegible]~~ 7MHz MODE

~~011~~ BACKGROUND CODE
000

3.58 MODE — 7MHz MODE.

100 ~~AN0~~ ACOLL0

101 ~~AN1~~ ACOLL1

110 ~~AN2~~ ACOLL2

111 ~~AN3~~ ACOLL3

AN1 AN0 VIDEO.
½ cck ½ cck → 1 COLOR CLOCK.

CODES FOR ANTIC
COLOR LUMINANCE REGISTERS
IN CTIA.

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

ANTIC INSTRUCTION DECODING

CODE	DESCRIPTION	VSIZE - 1	DMA RATE	GTIA CODES	SR CLOCK
0000	BACKGROUND N LINES	IRG, 5, 4	NA —	BACKGROUND	NA —
0001	JUMP	ϕ	NA —	BACKGROUND	NA —
0010	40 CH UC	8	40	7MHZ PAIRS (INVERTED OR BLANKED)	3.58 MHZ ×2
0011	40 CH U/LC	10	40	7MHZ PAIRS (INVERTED OR BLANKED)	3.58 MHZ ×2
0100	20 CH × 4 Color ×1	7	60/40	3.58 MHZ PAIRS	3.58 MHZ ×2
0101	" ×2 LINES	15	60/40	3.58 MHZ PAIRS	3.58 MHZ ×2
0110	20CH × 5 COLOR ×1	7	40/20	3.58 MHZ BITS GATING 2 BITS.	3.58 MHZ ×1
0111	×2 LINES	15	40/20	3.58 MHZ BITS GATING 2 BITS	3.58 MHZ ×1
1000	MM 40 CELL ×4	7	10	3.58 MHZ PAIRS	.9 MHZ ×2
1001	MM 80 CELL ×2	3	10	3.58 MHZ BITS	1.8 MHZ ×1
1010	MM 80 CELL ×4	3	20	3.58 MHZ PAIRS	1.8 MHZ ×2
1011	MM 160 CELL ×2 (×1 LINES	1	20	3.58 MHZ BITS	3.58 MHZ ×1
1100	MM 160 CELL ×2 (×1 LINE)	ϕ	20	3.58 MHZ BITS.	3.58 MHZ ×1
1101	MM 160 CELL ×4 (×2 LINES)	1	40	3.58 MHZ PAIRS	3.58 MHZ ×2
1110	MM 160 CELL ×4 (×1 LINE)	ϕ	40	3.58 MHZ PAIRS	3.58 MHZ ×2
1111	MM 320 CELL ×2 ×1 LINE	ϕ	40	7.16 MHZ PAIRS	3.58 ×2

WRITER	DATE	WITNESS	DATE
DECUIR	1/SEP/82		

GAME OR PROJECT

ANTIC VIDEO ENCODING DETAILS.

CONTINUED FROM PREVIOUS PAGE.

BLCH ≙ BLANK CHARACTER ENABLE
INCH ≙ INVERT CHARACTER ENABLE
TCCINA

LOGIC EQUATIONS FOR AU2, AU1, AUΦ

~~FROM PREVIOUS~~ ALWAYS. Φ11 FORCED IN DISPLAY, 0 IN H BLANK

AU2	AU1	AUΦ
Φ	Φ	Φ
Φ	Φ	Φ
1	$[SR7 \cdot (\overline{CH7 \cdot BLCH})] \oplus (CH7 \cdot INCH) \cdot \overline{LCINH} \cdot \overline{UCINH}$	$[SR6 \cdot (\overline{CH7 \cdot BLCH})] \oplus (CH7 \cdot INCH) \cdot \overline{LCINH} \cdot \overline{UCINH}$
1	$[SR7 \cdot (\overline{CH7 \cdot BLCH})] \oplus (CH7 \cdot INCH) \cdot \overline{LCINH} \cdot \overline{UCINH}$	$[SR6 \cdot (\overline{CH7 \cdot BLCH})] \oplus (CH7 \cdot INCH) \cdot \overline{LCINH} \cdot \overline{UCINH}$
SR7+SR6	SR7	SR6 + SR7·CHΦ
SR7 +SR6	SR7	SR6 + SR7·CHΦ
SR7	SR7 · CH7	SR7·CH6
SR7	SR7·CH7	SR7·CH6
SR7+SR6	SR7	SR6
SR7	Φ	Φ
SR7 +SR6	SR7	SR6
SR7	Φ	Φ
SR7	Φ	Φ
SR7+SR6	SR7	SR6
SR7 +SR6	SR7	SR6
1	SR7	SR6

WRITER	DATE	WITNESS	DATE
DECLAN	SEPT 78		

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

ANTIC INSTRUCTION DECODE - ANALYSIS, REDUCTION.

(NOT NECESSARILY MINIMAL)

WRITER	DATE	WITNESS	DATE

GAME OR PROJECT

~~ANTIC~~ ANTIC PINOUT

PIN COUNT 16 FEB 78

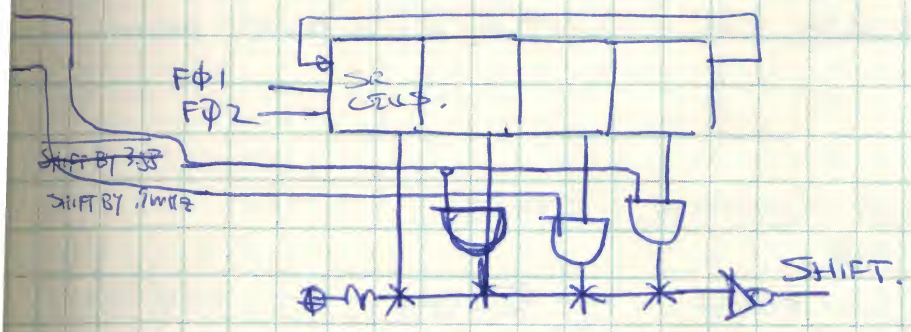
2	Vcc, USS
3	OSC, ϕ_0, ϕ_2
4	R/W, $\overline{HALT}$, $\overline{NMI}$, $\overline{RES}$
8	DB7-ϕ
16	AB15-ϕ
4	CSYN, AU2,1,ϕ
1	REF
1	LP
39	PINS.

POSSIBILITIES. EXCHANGE (RDY) FUNCTION ON CIA FOR (CSYN) FUNCTION ON ANTIC.

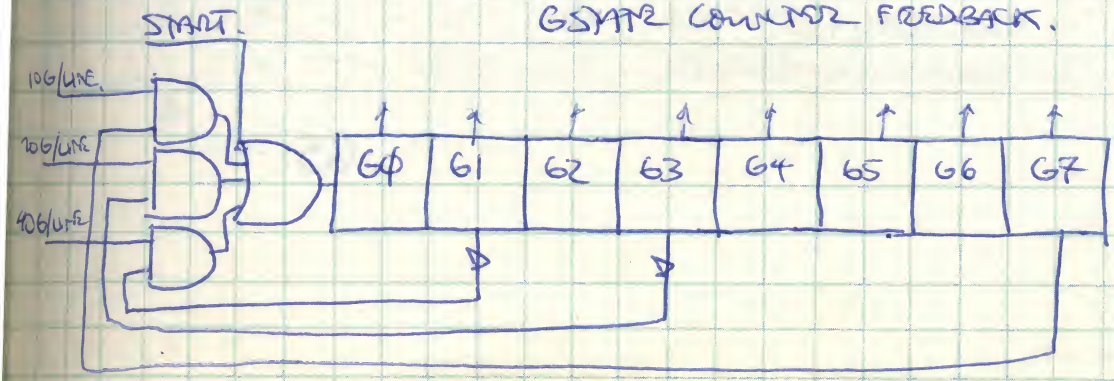
AD ADDRESS DECODE FOR POKEY

~~GSHIFT COUNTER~~

SKETCH. OUTPUT SR CLOCK GENERATOR.



GSHIFT COUNTER FEEDBACK.



WRITER	DATE	WITNESS	DATE
DECUIR			

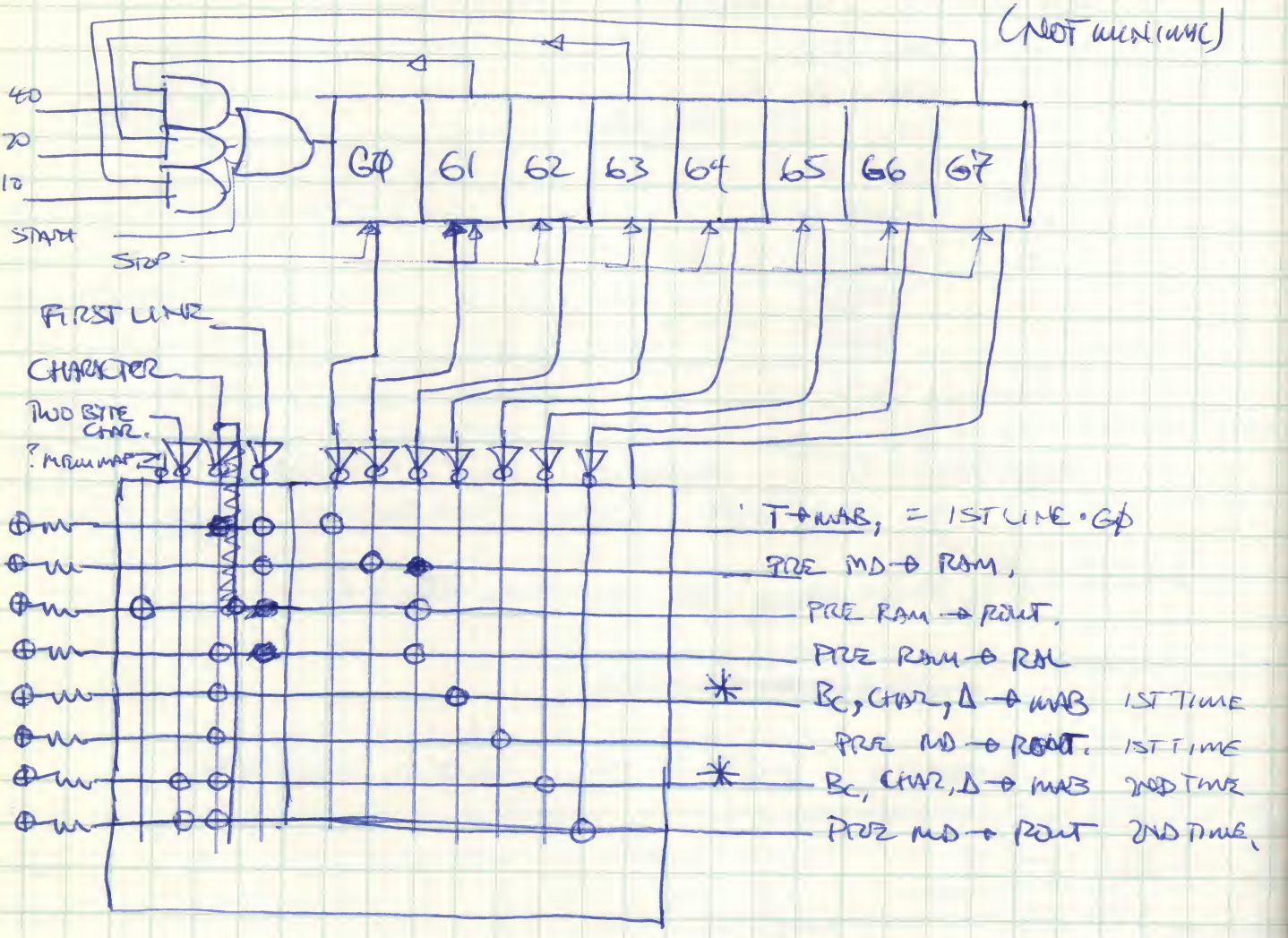
ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

ANTIC INSTRUCTION DECODE LOGIC, CONT.

FIRST CUT 6 STATE COUNTER COMMAND PLA

(NOT MINIMIZED)



* QUESTION, SHOULD SEPARATE STROBES BE GENERATED FOR:

40 CHARACTER FETCH.
20 CHARACTER/5 FETCH.
20 CHARACTER/4 1ST FETCH.
~~20 CHARACTER/4 2ND FETCH.~~

— ~~CB2~~	CH6	—	CH0	Δ2·Δ1	Δ0
— CB1	CH5	—	CH0	Δ2Δ1	Δ0
— CB3	CH7	—	CH1	0	Δ
— CB3	CH7	—	CH1	1	Δ

G5

BEING IN 1ST LINE
40 CHAR
20/4
20/5
MEM MAP.
+ G0-G6

WRITER	DATE	WITNESS	DATE
JOSEPH DECUIR	16 FEB 78		

GAME OR PROJECT
ANTIC.

FRANCOIS. IDEA.

USE 6Φ – 67

FOR FETCHING MISSILES & OBJECTS & INSTRUCTIONS.

6Φ 61 62 63 64 65 66 67

I_1 MS O1 O2 O3 O4 I_2 I_3

~~MOVE I_1 TO COUNT (2) (INSTEAD OF~~

LEAVE I_1 AT HSYNC = 2.

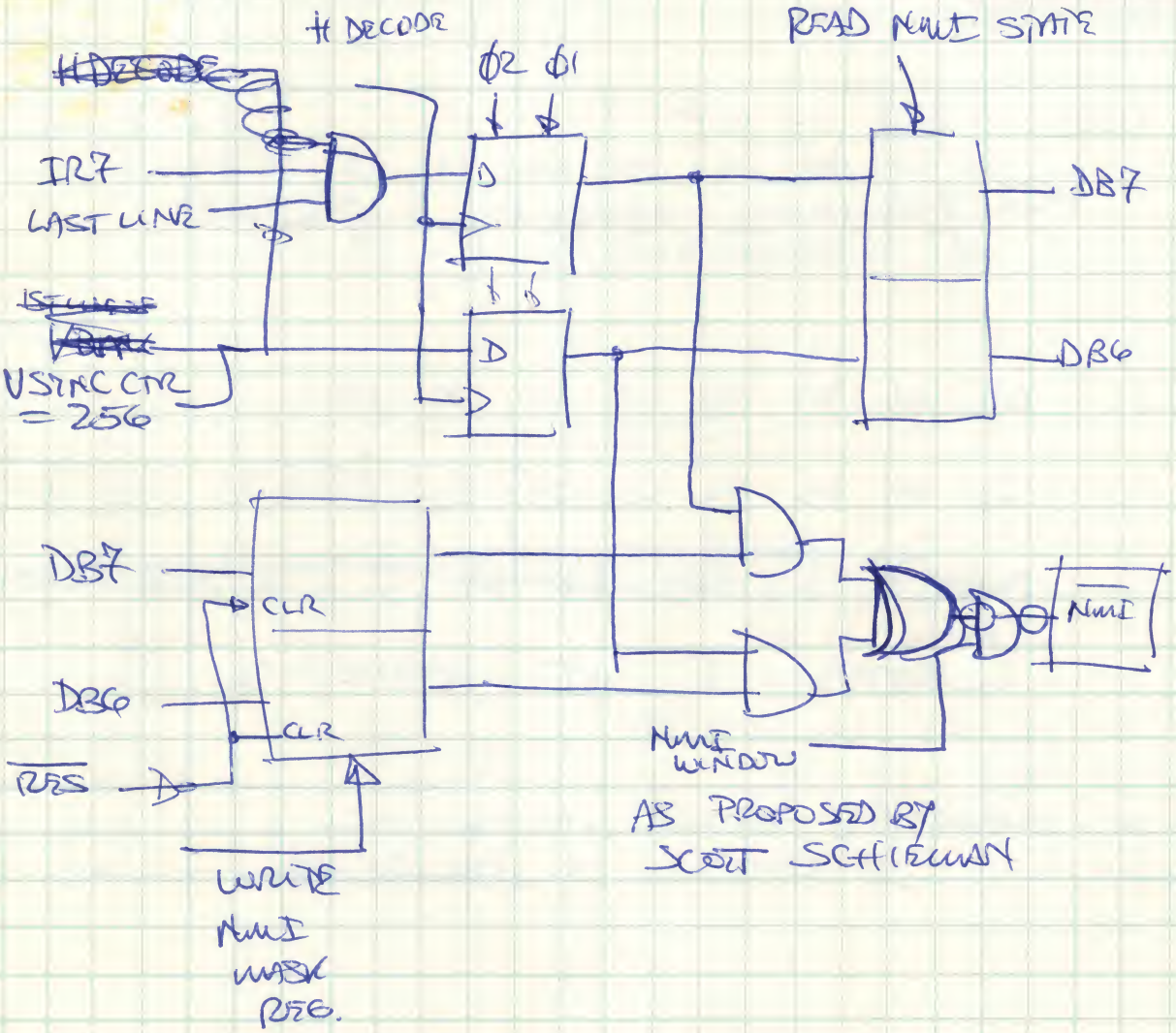
~~FORGET~~ ABOUT INHIBITING DMA CYCLES IN HSCROLLING.

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

ANTIC. NMI LOGIC.

TWO CONTROVERSIES, AND DECISIONS.



AS PROPOSED BY JOE SCHIEMAN

OKAYED BY JAY 23FEB,

WITH COMMENT ABOUT

1) MAKING NMI WINDOW ALWAYS SPAN SOME NON HALTED CYCLES - COULD BE WHOLE LINE

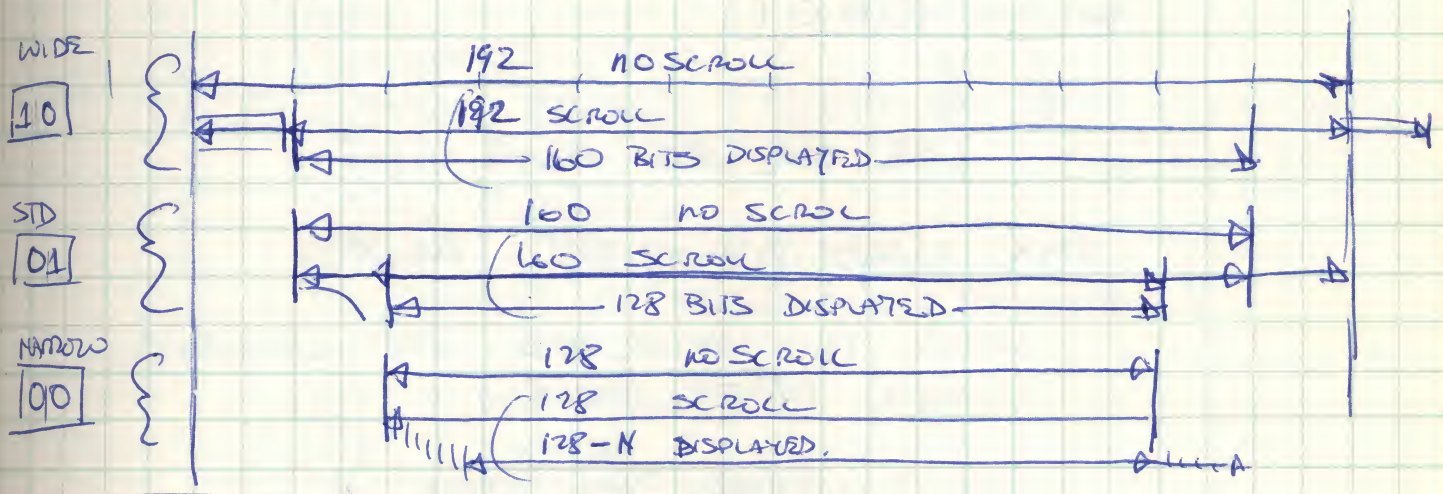
2) THE TWO REQUESTS MAY NOT NEED TO BE SAMPLED. - JUST DEGLITCHED.

WRITER JOE DREHER	DATE	WITNESS	DATE

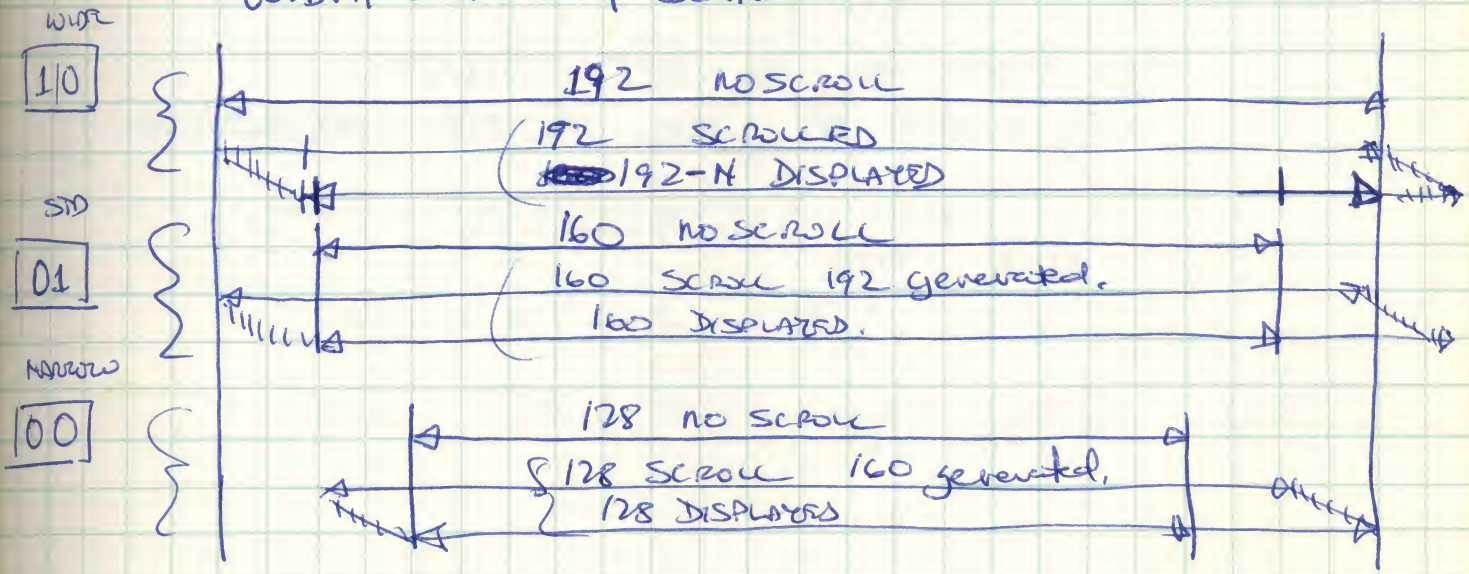
GAME OR PROJECT
ANTIC, HORIZONTAL SCROLLING/DISPLAY SIZE

TWO POSSIBLE CONVENTIONS.

USE TWO BITS OF HCONTROL REG TO SPECIFY WIDTH OF MEMORY SCAN SIZE AND MAKE DISPLAY IMAGE THE VARIABLE.



ALTERNATE PROPOSAL. TWO BITS SPECIFY WIDTH OF DISPLAYED DATA
WIDTH OF MEMORY SCANNED IS DEPENDANT VARIABLE



CONSENSUS OF JAY, FRANCOIS, HOWARD, SCOTT, LARRY KAPLAN, AND BOB WHITEHEAD ALL PREFER THE 2ND OPTION — HOWSE, IT SHALL BE ...

WRITER Dreimer	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
ANTIC

HOW IDEA FROM JAY MINER

JUMP INSTRUCTION

NMI	XX X	0001

USE ONE BIT AS A HALT.

MEANS LOAD DISPLAY LIST COUNTER

WITH THIS VALUE AND STOP COUNTING UNTIL NEXT VSYNC.

CALL IT WAIT FOR VSYNC

WVSYNC

SO THAT A 16 BIT INSTRUCTION IN FRONT OF JMP IS NOT NECESSARY,

USE DLI

WRITER	DATE	WITNESS	DATE
	2/28/78		

GAME OR PROJECT
CANDY / COLECO

SUGGESTED DEMO SOFTWARE FOR JAY

1. CHESS
2. BASIC
3. DESIGNER OS
4. 2 ACTION GAMES (EX: 4 PLAYER TANK, SUPERBUG)
5. INCOME TAX PROG. (?) (PERSONAL FINANCE)
6. MENU PLANNING
7. DEMON STATION CARTRIDGE (POINT OF SALE)
8. SUPPORT OF FOLLOWING PERIPHERALS
   a) PRINTER
   b) FLOPPY DISK
   c) CASSETTE
   d) DOSETT SYSTEM.

22FEB78

FROM MEMO BY KAPLAN 17FEB78.

JAY REQUESTS AN

APPLICATIONS NOTE ON

HOW THE ANTIC CAN STAND ALONE.

WRITER JOE DECUIR.	DATE	WITNESS	DATE

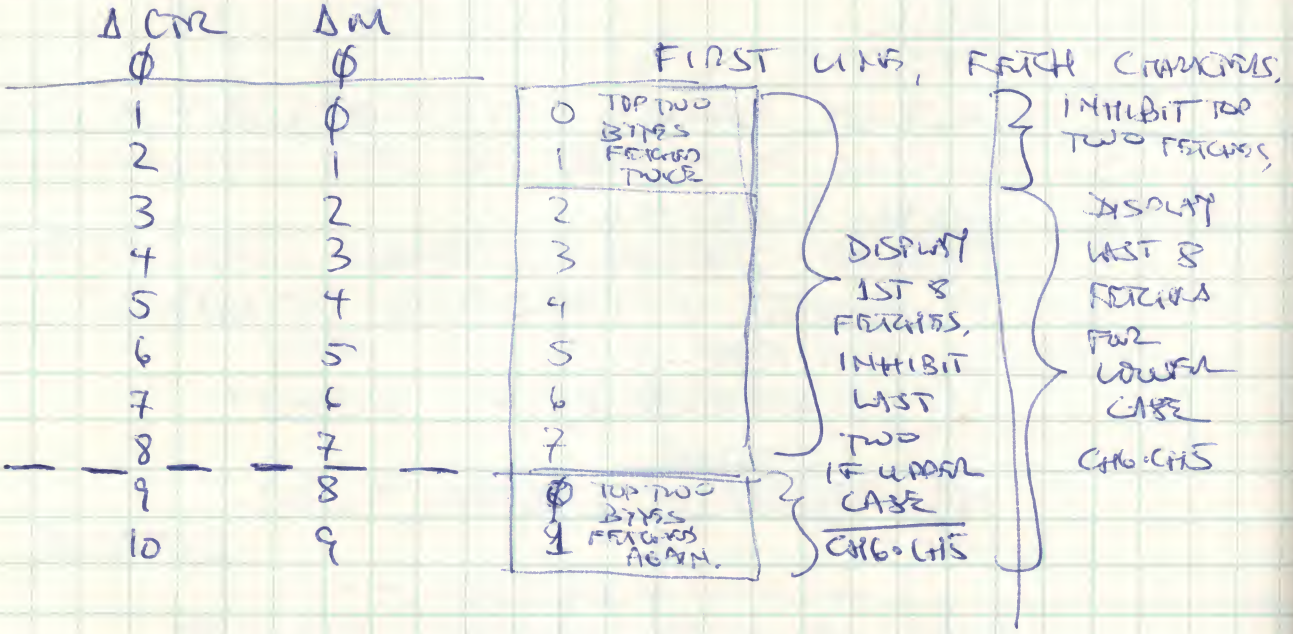
ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

ANTIC. U/L CASE CHARACTERS,

UPPER/LOWER CASE CHARACTERS. IRB-0 = 0011

ARE A SPECIAL PROBLEM.



· CONSENSUS W/ FRANCOIS IS TO DO THE INHIBITION IN THE OUTPUT PLA, WHERE CH6 AND CH5 ALREADY EXIST.

2MARCH, SIMPLE TRICK,
MOVE USYNC FUNCTION FROM
TIA2 TO ANTIC. AND TRY
IMPLEMENT IT WITH THE ~~FAST~~ LINE.

FRANCOIS's IDEA.

WRITER	DATE	WITNESS	DATE
SEE DRUM			

GAME OR PROJECT
ANTIC

~~CANTIDE~~ – ~~[redacted]~~

I HAVAN'T WRITTEN MUCH IN THIS NOTEBOOK FOR A WHILE, INSTEAD WORKING ON VERILOGS.

CHANGES TO DOCUMENT IN THE NEXT FEW PAGES:

1. PROPOSED CHANGES TO CHARACTER FORMATS OF ANTIC. (W CALCULATIONS
2. PROPOSED CHANGES TO NMI LOGIC, ESPECIALLY AS IT EFFECTS THE PROPOSED "RESET" BUTTON
3. PROPOSAL GIVEN TO BOB BROWN RE MUSIC SYNTHESIZER ~~CHIP~~ SYSTEM, AND "AIA" CHIP.

---

1. PROPOSED CHANGES IN CHARACTER FORMATS.

AFTER REVIEWING THE ANTIC DESIGN W/ ALBAUGH AND STUBBEN & CAIN-UP, AND REVIEWING ANTIC COMPETITIVELY W/RESPECT TO OTHER MACHINES, SPECIFICALLY THE PET, IT BECAME CLEAR THAT THE BLANK LINE AT THE TOP OF EACH LINE OF 40 CHARACTER TYPE DATA IS VIEWED AS A SEVERE LIMITATION IF THIS MODE IS TO BE USED FOR ANYTHING OTHER THAN ALPHA NUMERIC TEXT.

SO . . .

WRITER DECUIR | DATE 15 MARCH 78 | WITNESS | DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
ANTIC CONTINUED

SO - THE ~~ISSUE~~ ISSUE IS RE RAISED ABOUT WHETHER OR NOT THE MPU CAN TOLERATE BEING HALTED FOR MOST OF A LINE. IF ON THE FIRST LINE, THE ANTIC DMA'S BOTH CHARACTERS AND CHARACTER ~~GRAPH~~ GRAPHICS, IT WOULD LOCK OUT THE MPU, AND ANTIC RAM REFRESH.

THE MPU WOULD BE HELD A MAXIMUM OF 48+48 CYCLES + 1 REFRESH CYCLE -

$$97 \times \frac{2}{3.579545\ MHz} = 54.2\ \mu sec. = \frac{1}{18450\ Hz}$$

IF THE DYNAMIC STORES NEEDS IN THE MPU CAN TOLERATE THAT - ~~WE CAN USE THIS ELIMINATE~~ WE CAN PROCEED TO EXAMINE THE CONSEQUENCES OF LOST REFRESH CYCLES TO THE DYNAMIC RAMS.

ORDINARILY, THE ANTIC GENERATES 5 REFRESH CYCLES / HORIZONTAL LINE. HENCE, THE REFRESH PERIOD FOR 64 ADDRESSES IS:

$$\frac{64}{5} \times \frac{228}{3,579545} = 815\ \mu sec. < 1000\ \mu sec\ spec.$$

FOR 4K DYNAMIC RAMS.

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ENGINEERING LOG SHEET

GAME OR PROJECT: ANTIC.

ACTUALLY, A WORST CASE WOULD BE

LINE X	59	60	61	62	(63)
X+1	0	1	2	3	4
X+2	5	6	7	8	9
. . .					
X+11	50	52	53	54	55 54
X+12	55	57	58	59	60
X+13	60	61	(62)	(63)	

16 CLOCK CYCLES

$$\frac{13 \times 228 - 16}{3.579545}$$ = 823.57 μsec.

SO FAR, SO GOOD.

BUT, SUPPOSE SOME OF THESE REFRESH CYCLES GET LOST – 4 CYCLES GET LOST EVERY 8TH LINE.

LINE X	59	60	61	62	(63)	
X+1						∅ } A FIRST LINE
X+2	1	2	3	4	5	
3	6	7	8	9	10	
4	11	12	13	14	15	
5	16	17	18	19	20	
6	21	22	23	24	25	
7	26	27	28	29	30	
8	31	32	33	34	35	
9						36 } A FIRST LINE
10	37	38	39	40	41	
11	42	43	44	45	46	
12	47	48	49	50	51	
13	52	53	54	55	56	
14	57	58	59	60	61	
15	62	(63)				

} CHARACTER GRAPHICS DMA ONLY. (lines X+2 – 8)

−3×16

$$\frac{15 \times 228 - 3 \times 16}{3.579545} = 942\ \mu sec.$$

STILL SAFE

IF NO VSCROLLING INCREASES THE "FIRST LINE" FREQUENCY.

WRITER: DECUIR. DATE: 13 MARCH WITNESS: DATE:

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
ANTIC.

A START OR END VSCROLL
COULD POSSIBLY DELAY
THE 64TH ADDRESS 4 MORE
REFRESH WINDOWS, OR -
CONTINUING THE DIAGRAM FROM p 39

LINE
X+13 52 53 54 55 56 } END VSCROLL ENDLINE.
X+14 57 } EXTRA FIRSTLINE
X+15 58 59 60 61 62
X+16 (63) L.

$$\frac{16 \times 228 - 5 \times 16}{3.579545} = 996,774$$

- JUST CUTS IT!!

NOW, THE ABOVE DISCUSSION PRESUMES THAT A FIRST LINE KNOCKS OUT ALL 4 REFRESHES. IF THE REFRESH WINDOWS ARE CHOSEN TO BE IN HORIZONTAL OVERSCAN, LESS WOULD BE LOST IF WE WERE NOT IN 48 CHARACTER MODE. - 40 WOULD SAVE 1 OR 2, 37 WOULD SAVE MORE. -
THIS WOULD IMPACT WHICH DECODES ARE CHOSEN FOR REFRESH REQUEST.

WRITER DEANE.	DATE 15 MAR 83	WITNESS	DATE

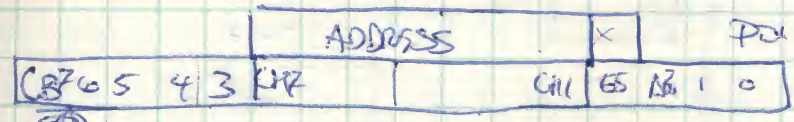
GAME OR PROJECT

ANTIC.

THE NEXT FALLOUT OF THIS DISCUSSION IS TO CHANGE THE "20/4" MODE TO A 40/4 MODE — MUCH MORE LIKE THE 40/2 MODE.

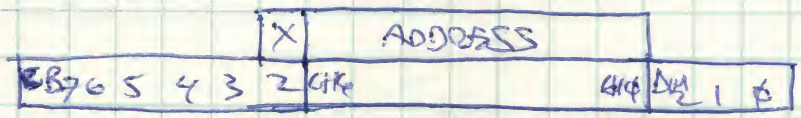
AS REQUESTED BY RON MILNER. STEVE WRIGHT, JAY MILNER, AND COLLEEN.

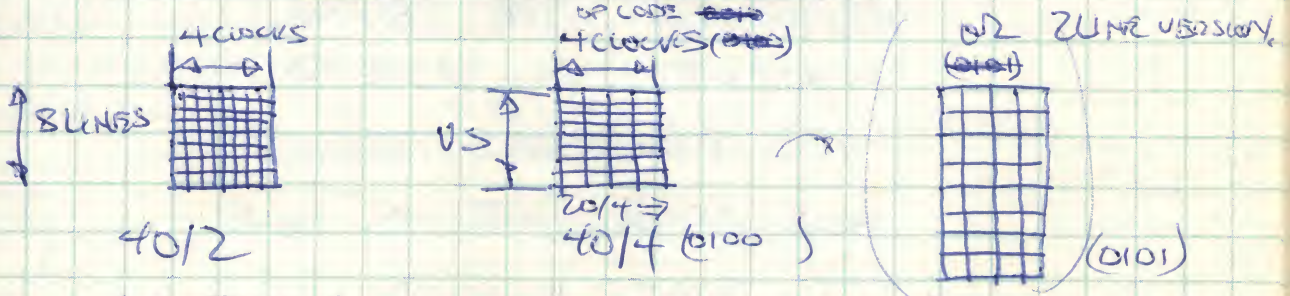
NOW, A 20/4 CHARACTER



CHARACTER, AND EACH LINE 2 BYTES HAVE TO BE FETCHED FOR EACH CHARACTER.

THIS COULD BE CHANGED TO THE SAME FORMAT AS 40/2





40/2

64 PIXELS, EACH $\frac{1}{2}$ CLOCK × 1 LINE × 1 BIT.

32 PIXELS / CLOCK × 1 LINE × 2 BITS

OR 32 PIXELS 1 CLOCK × 2 LINES × 2 BITS.

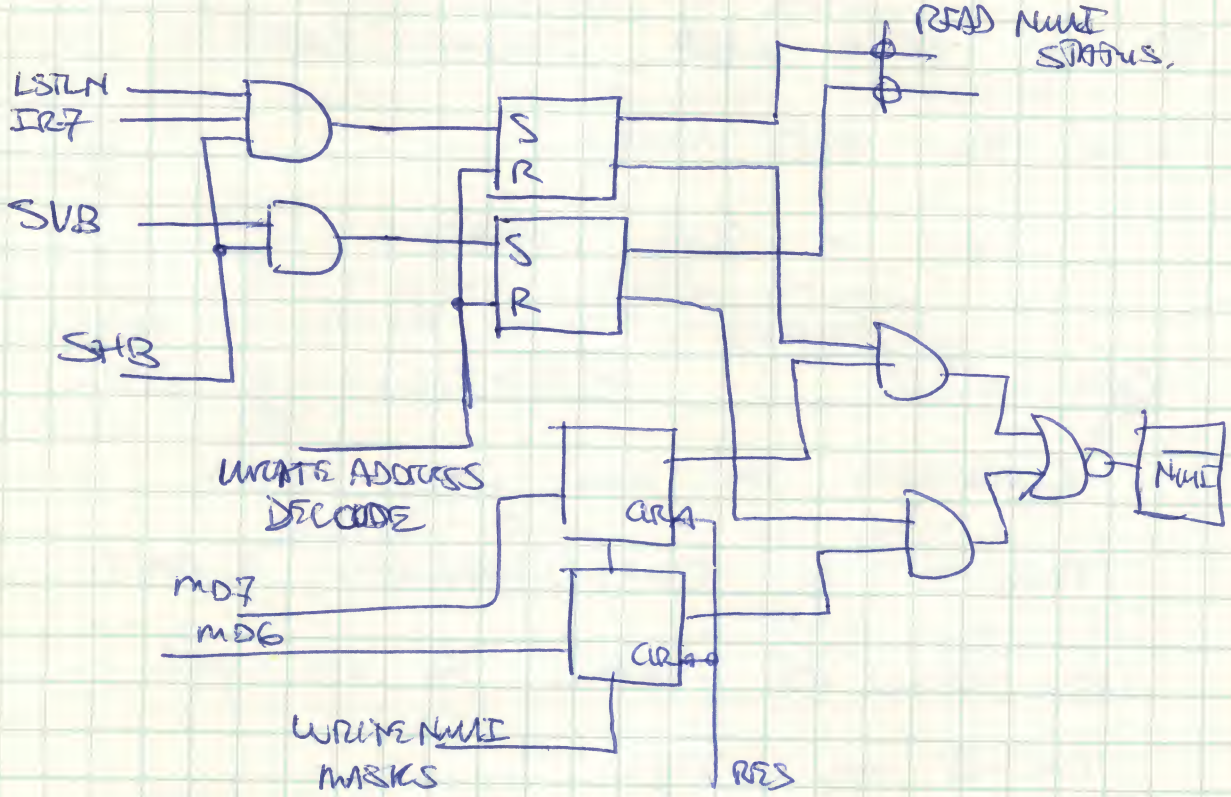
WRITER	DATE	WITNESS	DATE
DEMER	MAR 78		

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
ANTIC, NMI LOGIC.

CHANGES PROPOSED.

(REFERENCE OLD LOGIC, p 32)



ADDITIONALLY, THE VBLANK INTERRUPT IS DISABLED UNTIL THE PROCESSOR ENABLES IT. — BUT ONCE THAT IS DONE — IT STAYS ENABLED.

WRITER DAVE | DATE | WITNESS | DATE

GAME OR PROJECT

POSSIBLE MUSIC SYNTHESIZER.

DETAILS GIVEN TO BOB BROWN.

SYSTEM: RICHARD DERUCKSON

6502A/Q (SAME AS COLLEEN)

POKEY AND PIAS (SAME AS COLLEEN)
FOR SCANNING KEYS,
OPERATING VARIOUS CONTROLS,

ROMS (SAME AS STELLA/COLLEEN)
FIRMWARE FOR MPU,

→ AIA'S CHIPS - AUDIO IMAGE CHIPS, - SEE BELOW.

VCO'S

COMPANDING D/A'S.

AIA CHIP, 28 PINS,

8 REGISTERS.

CTRL . . . . .
÷M
÷N
÷O
÷K
VOLUMN
IMAGE INDEX
IMAGE DATA

REGISTERS.

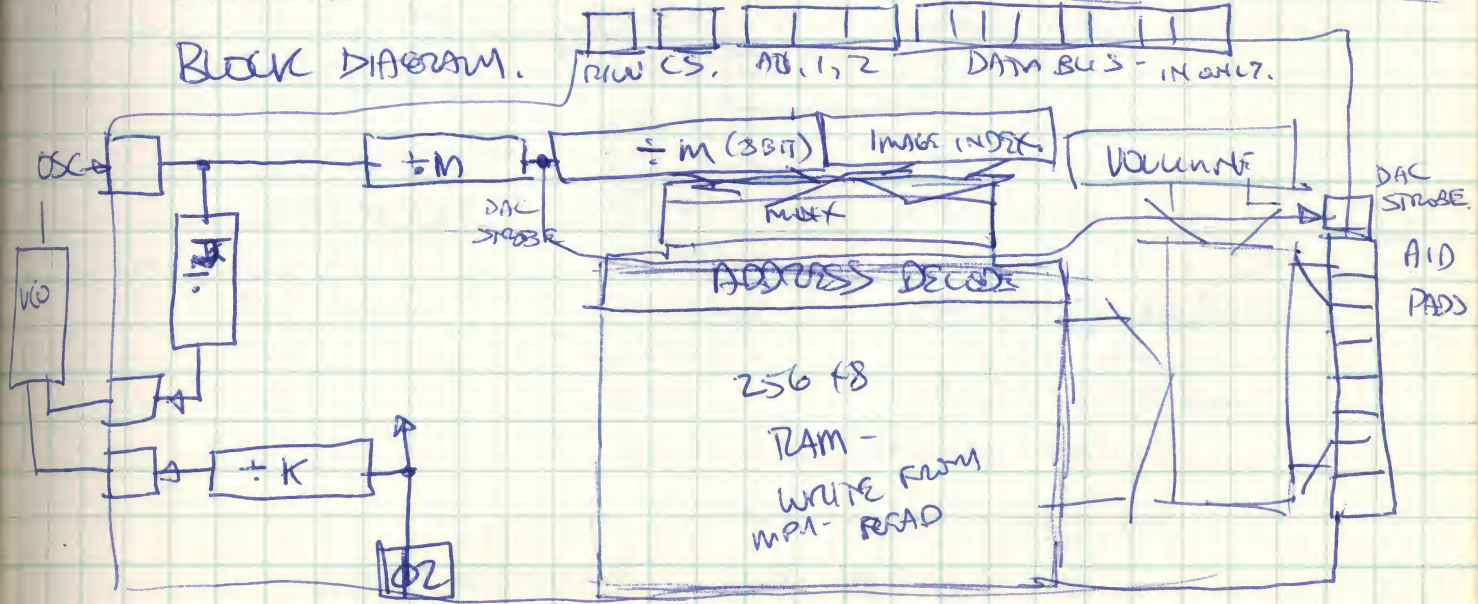
READ AND WRITE?

VSS, VCC	2	
Φ2, OSC	2	4
~~Φ2, OSC~~ OSC/2	2	6
DØ-D7	8	14
R/W	1	15
AØ, A1, A2, CS,	4	19
~~A3~~ AIDØ7	8	27
DAC STROBE	1	28
	28 PINS.	

~~A3~~ - PERHAPS - NO READ ADDRESSES,

BLOCK DIAGRAM.

R/W CS. A0, 1, 2 DATA BUS - IN OUT.



WRITER	DATE	WITNESS	DATE
DERUCK	17 MARCH 78.		

ATARI ENGINEERING LOG SHEET

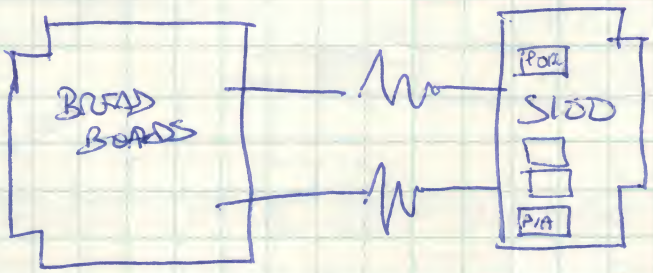
GAME OR PROJECT
DEVELOPMENT SYSTEM MEETING W/ GV,

~~CONCLU~~

INTERMEDIATE DECISIONS

GV DOES Z-2 BOX
BOARD SET, INCLUDING
6502 BOARD, AND
EVENTUALLY - THE TRACE
MEMORY.

DAN'S GROUP'S JOB IS
THE INTERFACE BETWEEN
THE TWO.



W/3 DUMMY SOCKETS.

CPU BOARD HAS
2 PIA'S, 2 ACIAS,
2K RAM, 2K PROM.
MULTIPLE CLOCKS SOURCES
HALT AND RDY LOGIC, - ELIMINATES M6502

WRITER JOSEPH DELENE | DATE 12/14/78 | WITNESS | DATE

GAME OR PROJECT

DEVELOPMENT SYSTEM.

ON CARD, - DOUBLE SIZE S100 WIRE WRAP CARD.

DB7-Ø
AB15-0
R/W
CØ2
Ø0
DRQ
NMI
RES
HALT
RDY

} ON CABLE.

IN FINAL PRODUCT. A NOVUS OF ATTIC.

2	VSS, VCC		POWER BUSSES
1	RES	RCVR	FROM EXTERNAL ONE SHOT
1	FØ0	RCVR	FROM CTIA
3	ANØ,1,2	1TTL e30pF	TO CTIA
1	CØ0	1TTL e30pF	TO MPU.
1	CØ2	RCVR	FROM MPU - ALSO TO LSTTL BUFFER CTIA AND
1	NMI	1TTL e30pF ?	TO MPU ?
1	HALT	1TTL e30pF	TO MPU
1	RDY	1TTL e30pF	TO MPU
1	R/W	RCVR	FROM MPU. W/CTIA, 1 BUFFER / AI4,15 (2 LSTTL BUFFERS BM)
16	AB0-AB15	1TTL e30pF	TO MPU, CTIA, LSTTL BUFFER
8	DB0-DB7	1TTL e30pF	TO MPU, CTIA, MOTHER BOARD.
1	REF	6LSTTL e	TO 3 RAM CARDS.
1	LP	RCVR	FROM MOTHER BOARD
1	CSYNC	~~1~~ 1TTL e30pF	NC

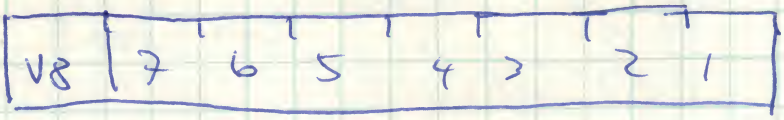
WRITER	DECUR	DATE 28MAR78	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
ANTIC.

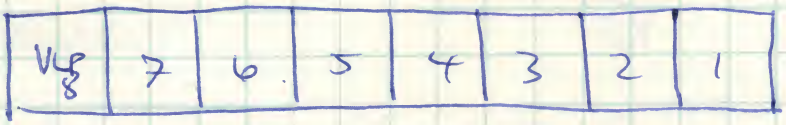
SUGGESTED CHANGE.

READ VERTICAL COUNTER.



DISCARD V0

READ VERTICAL LIGHT PEN.



DISCARD VLP0.

AGREE W/ FRANCOIS & JAY

WRITER | DATE | WITNESS | DATE

GAME OR PROJECT
6801.

MC 6801 - FAB IN LAYOUT NOW.

FAULT SAMPLES JUNE.

→ MIDSUMMER MORE LIKELY ESTIMATE FOR SAMPLES.

3870, REAL -
8048 - REAL -
6600 - DEAD
MC6801 - BUSH - W/ FAB RUN VERSIONS.
→ Z8 - BUSH
65816 - ? MYSTERY.
9940 - REAL

SAMPLING MONTH OR TWO BEHIND 1680

INVESTIGATE MC6809 FOR COMPATIBILITY W/ NEW M+M.

68488 IN PRODUCTION !!!!

6801 ~ 300mil CHIP FAMILY.

WRITER | DATE | WITNESS | DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
COIN-OP PERIPHERALS.

ROCKWELL 6500/1.

6502 CPU EXACTLY CALLING.

2K BYTES ROM
64 BYTES RAM MAPPED INTO
00-3F DOUBLE MAPPED
100-13F

STAR BUCK
714-632-3880

I/O INPAGE 3500. 80-8F

80 — 8 BIT PORT ALL IDENTICAL
81 — " "
82 — " "
83 — " "

ALL (6 K) PULLUPS —
WRITE 1's.
MASKED — REMOVE 8 PULLUPS
AT A TIME.

PA Φ, PA1 LINE — EDGE DETECT CKTS.

WRITE
84 } 16 BIT COUNTER UPPER
85 " " " LOWER
READ
86 }
87 }

88 LOAD UPPER LATCH AND DOWNLOAD TO CTR

TIMER INTERRUPTS
— LOAD AND COUNT DOWN
— GENERATE EXTERNAL PERIOD.
— COUNT EXTERNAL PERIOD
— COUNT EXTERNAL FREQ

WRITER [illegible] DATE WITNESS

GAME OR PROJECT
CONSOLE PERIPHERALS.

8A CLEAR PA1 STATUS
8A " PA0 "
B
C
D
E
} UNUSED

2ND SOURCE AGREEMENT W/ SYNERTEK

8F CONTROL REGISTER

D0
D1
} CLOCK MODES

D2 PA0 INTERRUPTS
D3 PA1
D4 TIMER

D5 PA0
D6 PA
D7 TIMER
} STATUS.

PERSONALITY BOARD FOR SYSTEMS W/ INCIRCUIT EMULATION

~~2MHZ PART~~
DRQ NOT BROUGHT OUT.
CAN USE PA0, PA1.

NMI IS BROUGHT OFF

34
40 1 FOR CLOCK INPUT (TO ~~CONSOLE~~ TIMER)

3 Vcc, Vss
RAM POWER

2 XTAL1, XTAL2

1 RES

40 PINS

2ND GO ROUND

$1 → $8 or 9

SAMPLING PART IN 3 WKS
EMULATOR 64 PIN.

WRITER DREW | DATE 3 MARCH | WITNESS | DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

MC6809 SEMINAR

BOB BURLINGAME from AUSTIN
APPLICATIONS.

DENNIS HABGOOD LOCAL µP & PERIPHERALS
FIELD APPLICATIONS ENGINEER

HASH PATEL LOCAL FACTORY REP

ERNIE BARBARO. SYSTEMS SALES MGR

COVERED BY NON DISCLOSURE AGREEMENT.

ASK ABOUT FAST FUNCTIONS

WANTS COMMENTS ABOUT
WRITEUP AND PRESENTATION.

1. TWO XTAL INPUTS. 4X BUS CLOCK.
or 2X BUS CLOCK
(PROGRAMMED BY RESET)
(AT RESET, DEPENDS ON FIRQ AND IRQ)

EXTERNAL, INTERNAL CLOCK ALSO CAUSES DRIVE Φ2 IN.

FIRQ - LIKE IRQ & MASKABLE PC AND STATUS ONLY SEPERATE VECTORS

RDY INPUT - STRETCHES Φ2
ON '09 STRETCHES Φ1 IF GOES LOW IN Φ1, OR STOPS DURING Φ2 IF TRANSITIONS DURING Φ2

WRITER	DATE	WITNESS	DATE
11 APRIL 78 DECKER			

GAME OR PROJECT
MC6809

~~HALT~~ INPUT — POSTPONE HALTING DISCUSSION UNTIL LATER.

HAS E BIT - SO THAT MACHINE KNOWS HOW MUCH OF MACHINE TO RECOVER (STATUS AND PC. OR WHOLE MACHINE)

TWO NEW SOFTWARE INTERRUPTS
SWI2
SWI3
SWI1 SNARFED BY MICROCOMPUTER DEVELOPMENT TYPES

SYNCH INSTRUCTION
CAUSES IDLE ~~STATE~~
~~BA~~ BA GOES HIGH.
RESET ~~IS ONLY~~
OR INTERRUPTS ARE ONLY EXIT.
(EDGE?)

NO TSC!!!
~~COULD USE~~

L.I.C OUTPUT. CYCLE BEFORE OF CODE FETCH.

VECTOR FETCH OUTPUT.
(FOR USE WITH AN INTERRUPT ENCODER CHIP - IN THE WORKS)

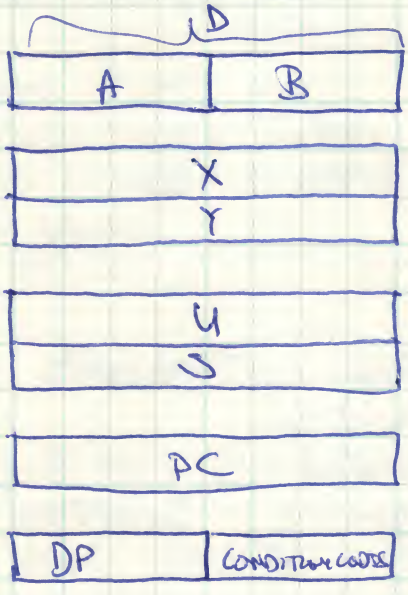
BUSY - FOR LOCKING OUT OTHER CPU'S WHEN DOING READ MODIFY WRITE

WRITER DREHER | DATE | WITNESS | DATE

ATARI ENGINEERING LOG SHEE

GAME OR PROJECT
MC6809

PROGRAMMING MODEL



INDEX

OR A or B, or D

X, Y, U, S, PC+ 5 BIT, 8 BIT, 16 BIT NUMBER

TWOS COMPLIMENT.

Pc ~~8 BIT OR 2B~~ 8 OR 16 BITS ONLY,

AUTO INCREMENT X, Y, S, U,

U DIFFERENT BECAUSE YOU CAN PUSH OR PULL ANY OR ALL REGISTERS WITH IT

~~INDIRECT ADDRESSING~~

2 BYTE INSTRUCTION

MANY INDEXED INSTRUCTIONS ARE ESSENTIALLY 2 BYTE.

WRITER	DATE	WITNESS	DATE
DECUIR	11 APR 78		

GAME OR PROJECT
MC6809

MANY, MANY INSTRUCTIONS ARE 2 BYTE.

SIGN EXTEND INSTRUCTION
(B INTO A)

THE HALF AND CARRY FLAG WILL STILL BE IN THERE

INDIRECT ADDRESSING

[X]

(X) → (EA) → DATA

THIS CAN BE DONE OFF THE SP or U!!!

IMM
DIR
EXTENDED
INDEXED
RELATIVE
} W/ W/O INDIRECT.

LEA !!! ex LEA Y D,X

means D+X → Y

{A, B & D, ±4, 7, ±15} + {X, Y, U, P, S} → {X, Y, U, S}

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
MC6809

INX AND DEX DISAPPEARED INTO LEA.
BECOME 2 BYTE.

MULTIPLY A×B → D
11 CYCLES!!! UNSIGNED.

NO DIVIDE.

SAME AS OK 6801
(TOM WANTED IT OK 6801!!!)

BCD - SAME AS 6800

DECIMAL HARDWARE EATS SPACE.

ADD AND SUBTRACT DOUBLE REGISTERS
IS DIFFICULT - DOES NOT ADD IN CARRY

PRODUCTION QUANTITIES WITHIN RANGE OF PRICE OF 6800 IN LATE QT. EARLY 2ND

PRODUCT SAMPLES AVAILABLE IN CARROLL
1ST SILICON SEPT
NOV 15.
SAMPLES IN JANUARY - MAYBE
CARROLL 2ND ON SIDE. THEN SHRINK.

30% SHRINK ON FIRST RUN.
(THEY WILL HAVE FUNCTION BOARDS IN 6 WEEKS
SIMULATION BY 6800)

WRITER DECUIR | DATE 12-21-77 | WITNESS | DATE

GAME OR PROJECT

MC6809

BREADBOARD NOT FINISHED

LOGIC SIMULATION DONE.

DEFINITION DONE BY MARKETING AND ENGRING.
AND PROGRAMMERS . . .

6809 DESIGNED FOR 90 nsec ~~from 150 nsec~~ [D1 to X ADDR BUS

SOME INSTRUCTIONS ARE FASTER.

~~STA USED TO BE SLOWER~~ (D)
~~TOOK EXTRA~~

TO SAVE THAT ADDRESS SETUP.

THEY SLOWED DOWN THE DIRECT AND EXTENDED INSTRUCTIONS!!

JUST DONE RECENTLY.

6805 X/2-3 6800 LESS B AC

CLOCK ON CHIP.
1K ROM.
64 RAM.
16 I/O LINES
1 TIMER.

} 24 PIN PACKAGE.
OFFSET Ø OR 16 BITS.

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
MC680X

MOTOROLA HAS THE CAPABILITY TO MODIFY THE 6800 TO HAVE THE $\overline{\text{HALT}}$ FUNCTION WE NEED IN A FEW MONTHS.

ADDRESSES ON ANTIC 12 APRIL 78

0	DMACTL	WR
1	CHCTL	WR
2	~~DLL~~ DLISTL	WR
3	~~DLH~~ DLISTH	WR
4	HSCROL	WR
5	VSCROL	WR
6	———	—
7	PMBASE	WR
8	———	WR
9	CHBASE	WR
A	WSYNC	WR
B	VCTR	RD
C	HLP	RD
D	VLP	RD
E	NMIEN	WR
F	NMIST / NMIRES	RD/WR

WRITER	DEAN	DATE	WITNESS	DATE

GAME OR PROJECT

KATIE

BILL BRIGGS MINER ASSAR, DOM SPRINGER

DAN MINER DAN SHEPPARD, STEVE MAYER

AL ALCORN, JOE DECUIR

1ST ADD 4 BREAK INSTRUCTIONS (JSRS)
BRP. 1, 2, 3, 4

2ND CHANGES.

ALL 8 TO 16 BIT TRANSFERS
IGNORE HIGH BYTE

16 TO 8 BIT TRANSFERS
IGNORE HIGH BYTE.

TO PROTECT TXS, AND CONSISTENCY

JSR, JMP MAYBE

CAN NOT GO IN !!!! MEMORY TO MEMORY !!!

DAN VERY OPPOSED TO LDQ SINGLE BYTE, !!!

PROPOSAL FOR SQA, CQA + LDQ (2 BYTE)

PROPOSAL FOR DOUBLE INCREMENT/DECREMENT.
BY 2, X = X ± 2 Y = Y ± 2

WRITER	DECUIR	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
KATIE (COPY)

2 REGISTER

MIKE STILL LIKES IT. DBZ.

CONTROVERSIES ABOUT AUTO INCREMENT
VS PURE INDIRECT.

- BACK TO PURE INDIRECT

WE MIGHT SUBSTITUTE DBX. DBY

JSR 8 BIT RELATIVE
(ABS)

COMPLETES A SET

JMP	ABS	(ABS)	REL16	REL8
JSR	ABS	(ABS)	REL16	REL8

LDP IM LOW PRIORITY

CHANGE TPY → PCY
TPP → YPC

FOR MULTIPLY,
ELIMINATE LSX ASX

ADD ROX, ROY [RLX, RLY]

WRITER	DATE	WITNESS	DATE

GAME OR PROJECT
KATIE (CONT)

ADD 3 LOAD IMMEDIATE HIGH BYTES
(INSTEAD OF SIGN EXTENSION)

8BIT A + 16BIT X → SIGN EXTEND 8
+16 → 16

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
COLLEEN. DEVELOPMENT SYSTEMS

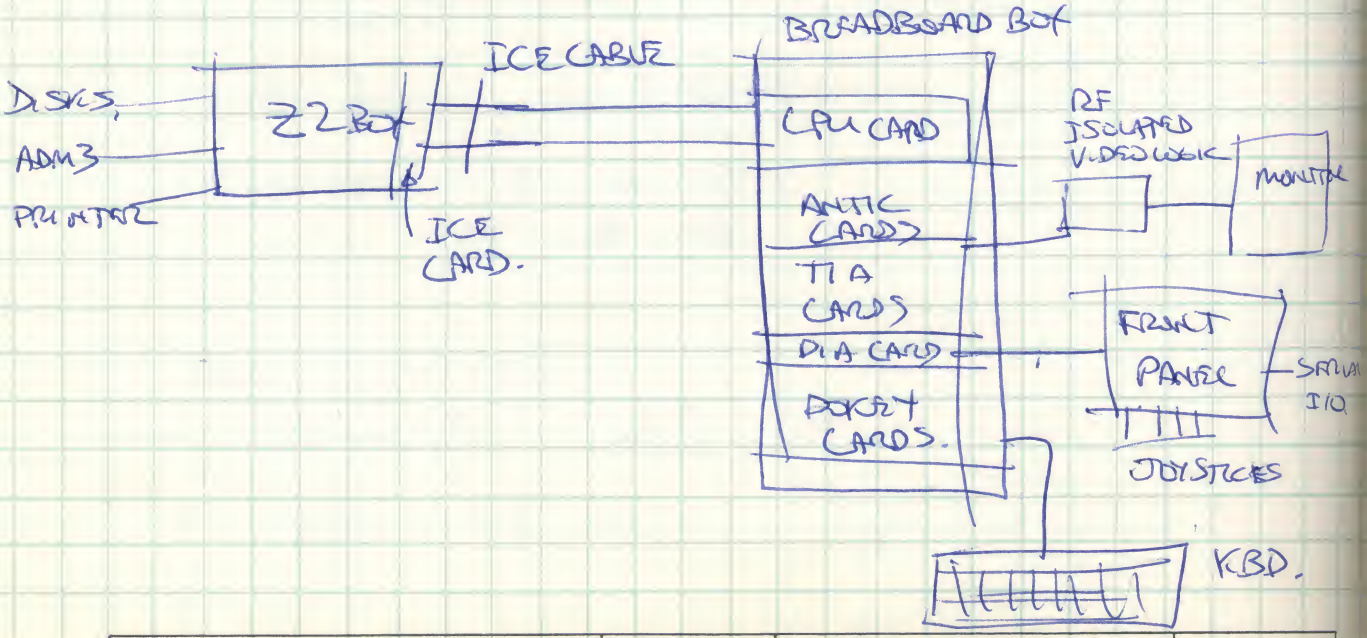
FOR CHIP DEVELOPMENT
TWO BIG CARD CAGES.

1) BREAD BOARDS.
14 SLOTS. 144 IC'S / CARD ANTIC, TIA, FOOEY (PIA)
100 PIN CONNECTORS
AB0-15, DB0-7, R/W, Φ2 } COMMON SIGNALS (+VSS, VCC)

2) CROMEMCO Z2 BOX (BUILT BY GRASS VALLEY)
20+ SLOTS.
100 PIN S100 TYPE BUS.
CPU BOARD
ROM, RAM
MONITOR I/O
TRACE BOARD.

PROPOSALS:

TWO STAGES OF DEVELOPMENT
1) CHIP DEVELOPMENT:



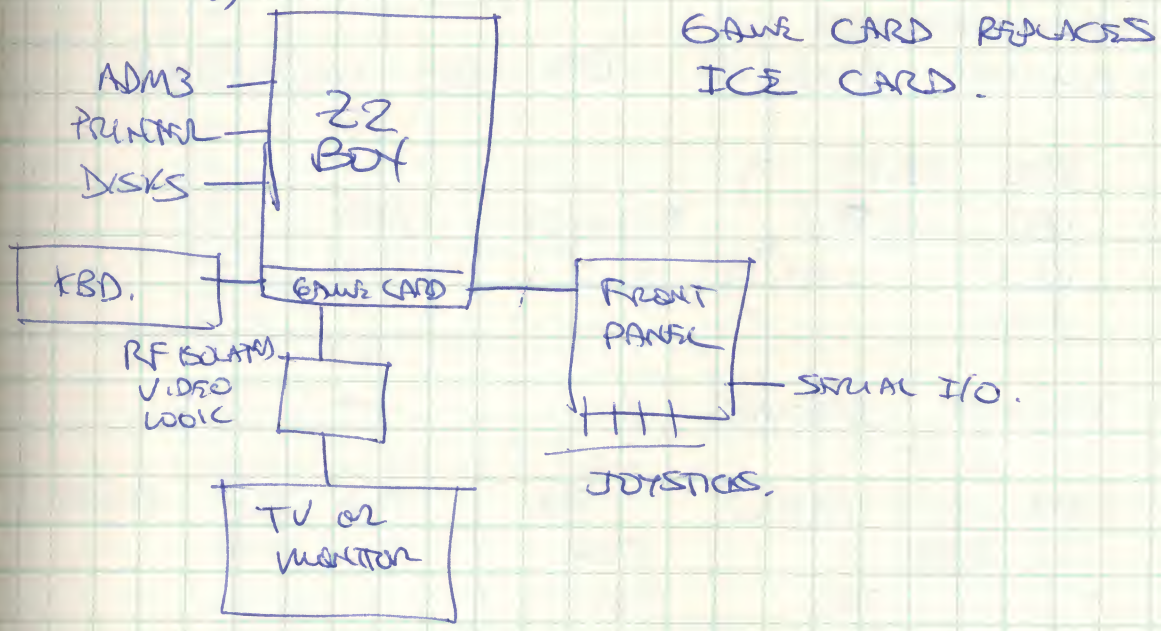
WRITER [illegible] DATE [illegible] WITNESS DATE

GAME OR PROJECT

COLLEEN DEVELOPMENT SYSTEMS

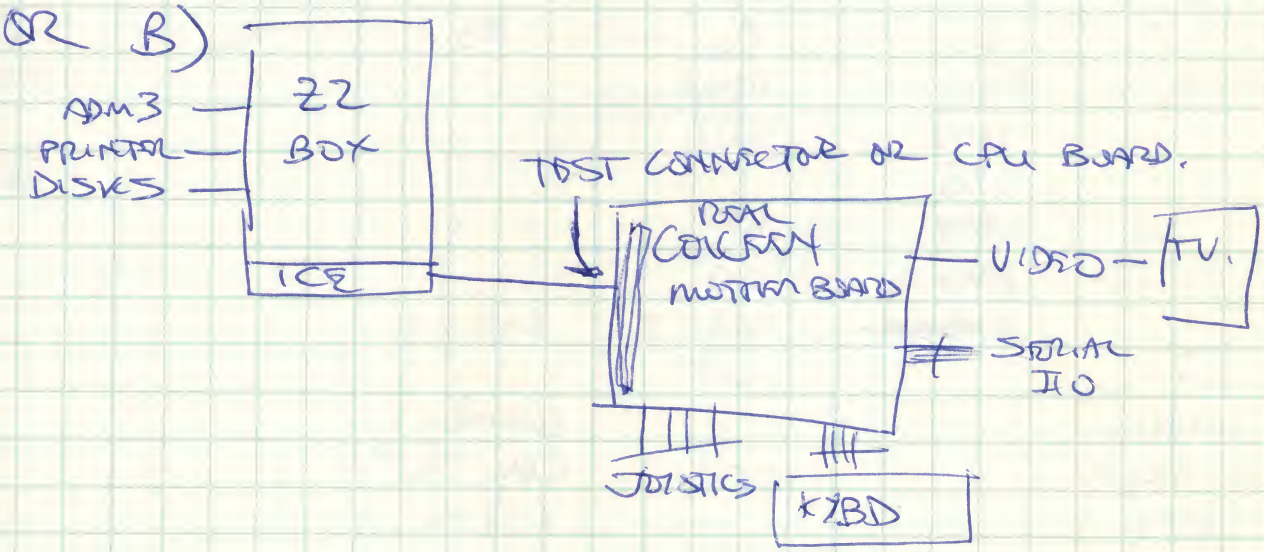
2) CHIPS WORKING.

A)



GAME CARD REPLACES ICE CARD.

OR B)



WRITER JOSEPH DECUIR	DATE APRIL	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

COLECO, DEVELOPMENT SYSTEM.

DETAILS:

~~SPECIAL SIG~~

COMMON SIGNALS ON BB BACKPLANE:

ABϕ - AB15
DBϕ - DB~~6~~7
R/W
ϕ2

} FROM CPU CARD

SPECIAL SIGNALS.

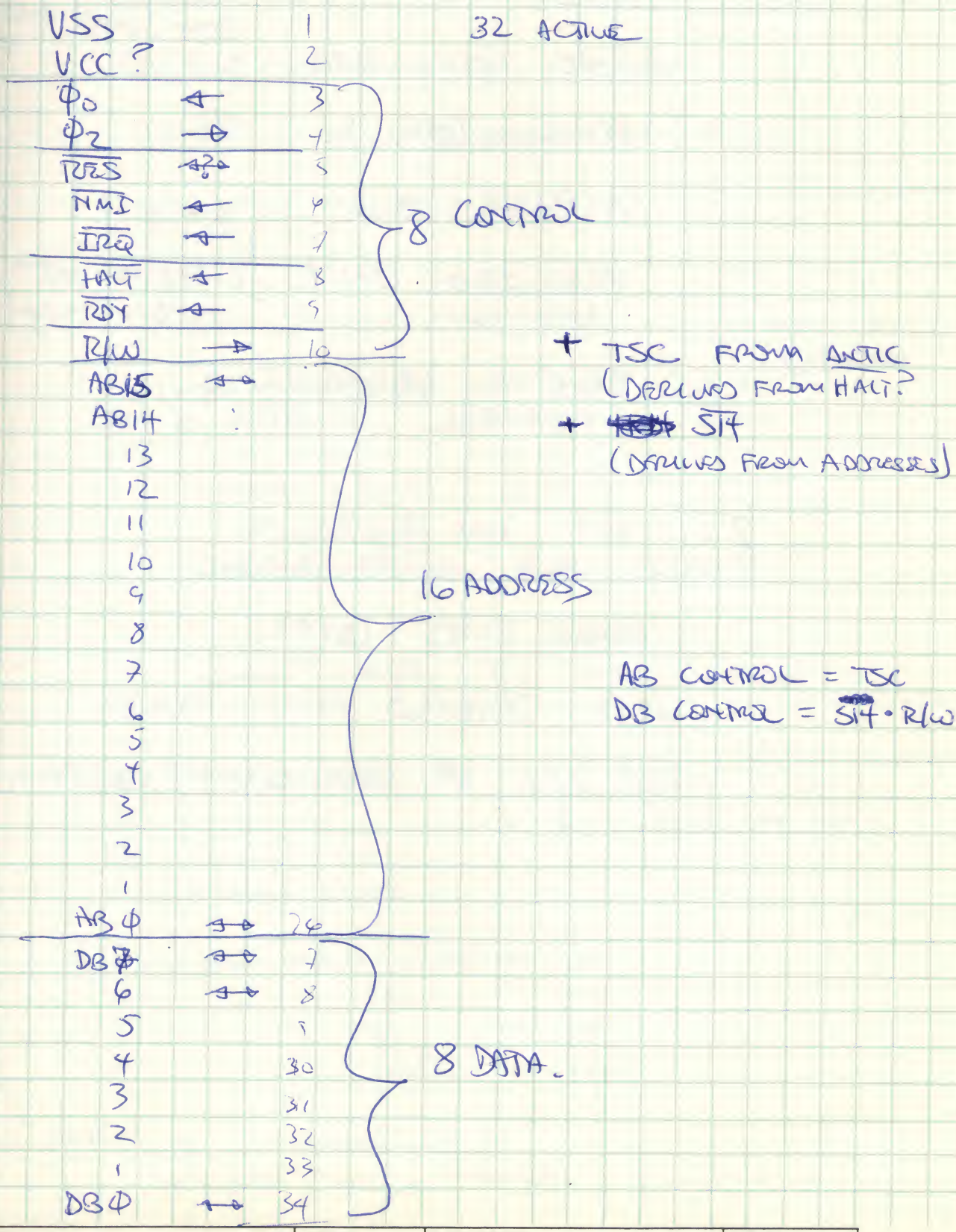
MAIN BOARD.	CPU	ANTIC	TIA	P.I.A	POKEY
OSC			OSC		
		Fϕ0	Fϕ0		
	ϕ_0	ϕ_0			
(	ϕ_2	ϕ_2	ϕ_2	ϕ_2	ϕ_2)
RESA, M	RESM	RESA			RESM
	$\overline{NMI}$	$\overline{NMI}$			
	$\overline{IRQ}$				$\overline{IRQ}$
	RDY	RDY			
	$\overline{HALT}$	$\overline{HALT}$			
	~~ANϕ1,2~~	ANϕ.1, 2	ANϕ.1, 2		
$\overline{LP}$		$\overline{LP}$			
LUMϕ.1, 2			LUMϕ1, 2		
COL, PAL, DEL		(REF)?	COL, PAL, DEL		
CSYNC			CSYNC		
Sϕ-3			Sϕ-3		
Tϕ-3			Tϕ-3		
PAϕ-7				PAϕ-7	
PBϕ-7				PBϕ-7	
CA2, CB2				CA2, CB2	
SCLK, SDO, SDI, SRQ					SCLK, SDI, SDO, S
POT ϕ-7					POTϕ-7
Kϕ-5, KR1,2					Kϕ-5, KR1,2
AUDIO.					AUDIO

WRITER JOE DECUIR	DATE 18 APRIL	WITNESS	DATE

GAME OR PROJECT

COLLEEN, DEVELOPMENT SYSTEM.

CPU TO BREAD BOARD INTERCONNECT.



WRITER	DATE	WITNESS	DATE
JOE DECUIR	18 APRIL		

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
Z8

Mel Snyder SALES MGR Z80A
~~HOOSON CO.~~
JEFF WARD THOMSON COMPANY.

Z8. LAYED OUT.

MASKS BEING MADE

UNDER 200 mils #/5

SAMPLES JUNE } 64 PIN
PRODUCTION JULY. } EXTERNAL
1000 UNITS. ROM VERSION

2ND SOURCE NEGOTIATIONS IN PROGRESS. MOSTEK IS ONE

Z8 not non disclosure
Z8000 also non disclosure

FASTER PARTS LATER.

PL/Z DERIVED FROM PASCAL

HARD DISK ~~IN~~ DEVELOPMENT SYSTEM

WRITER JOSEPH DEGEN	DATE	WITNESS	DATE

GAME OR PROJECT

MEETING W/ CIRCUIT DESIGNERS RE ELECTRICAL SPECS

VOLTAGE SPECS FOR PINS.

OUTPUT / INPUT 1-0 LEVELS

INPUT 1 IS ~~2.4 VOLTS~~ derived from IS 2.4 VOLTS } from MP SPECS

INPUT Φ IS 0.4 VOLTS, }

LOGIC 1 INPUT IS 2.0 } from SCOTT. ~~ANTIC~~

LOGIC Φ INPUT IS 0.8 }

OUTPUT LEVEL 2.4 } from MP. and SCOTT.

OUTPUT LEVEL 0.4 }

SCOTT WANTS .4V NOISE MARGIN

SPECIAL CASE — $F\Phi_0$ CTIA → ANTIC (depletion pullup.)

Φ_0 ANTIC → MPU

$F\Phi_0$ 2.4v, 0.4 output
2.0v., 0.8 input

WORST LOADS (CHIP TO CHIP)

$F\Phi_0$ - AN Φ, 1, 2

Φ_0 RDY

NMI HALT

64 DATA BUS 1000 ~~μm~~ microns CHANNEL LENGTH ~~outside~~. (25μ/mil)

WRITER JOE DECUIR	DATE 20 APRIL 78	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
CKT DESIGN MEETING

ACTION REQUESTS.

1. DSC — NILES
2. OUTPUT DRIVR — SCOTT
3. TIMING. — SCOTT ET AL
4. CURRENT — SCOTT
5. SYSCKT — SCOTT
6. FAST FP. — SAM
7. LEVELS.
8. COMP SPEED — CARL

LISA LOOP

CONSULTANT OF USES OF COMPUTERS IN EDUCATION.

"SELF MOTIVATING LEARNING SYSTEMS"

WALKING & TALKING ARE HARDEST.

LEARNING IN WESTERN CULTURE
HOME & FAMILY
SCHOOL CURRICULUM
STREET LEARNING (including video games)
VOCATIONAL TRAINING
RECREATION

WRITER	DATE	WITNESS	DATE
20APRIL78, DSC			

GAME OR PROJECT
LIZA LOOP

TRADITIONAL SOCIETY

⇒ GLOBAL VILLAGE
LIFE LONG LEARNING
FLUID ROLES
UNPREDICTABLE ROLES
LESS THAN ON GENERATION.

MASS MARKET:

EDUCATIONAL
psycho motor development
problem solving techniques
specific content

RECREATION
sports and games
creative arts
media (Spectative) (reading, music, tv, watching stuff).

ATARI PRODUCTS
video games
computer games & programming
CAI
artistic programming audio or visual.

(she sees computers being used to provoke participation)

NO CLEAR DIVIDING LINE BETWEEN WORK AND PLAY.

WRITER	DECUIR	DATE	20 APR 78	WITNESS		DATE	

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
LISA LOOP (CONT)

MURPHY DILEMMA

PROTESTANT ETHIC VS TECHNOLOGICAL ETHIC

PEOPLE MUST WORK

MACHINES MUST WORK
PEOPLE MUST PLAY.

WHAT MAKES GAMES INTERESTING

COMPLEXITY, SKILL, THEME

learning acquired thru vocational games has prevocational value
learning acquired through play games has unknown value

---

complex multiplayer games very popular
talked about PLATO - dogfight games.

GAME IS EDUCATIONAL IF IT IS A

SAFE AND SIMPLIFIED SIMULATION
of A
REAL WORLD SITUATION.

WRITER [illegible] | DATE [illegible] | WITNESS | DATE

GAME OR PROJECT
LIZA LOOP

WHERE TO GO FROM HERE?

1). USE game components to systematically enlarge prepackaged game library for recreation.

2) USE vocational analysis for marketing prepackaged games to parents and schools

3) Develop a Game Writers application language for the home computer using theme-skill-complexity variables

(best books are ones you wish you had written yourself)

LIZA'S DREAMS

USE ATARI TECHNOLOGY to RECONSTRUCT OR EXISTING FORMAL EDUCATIONAL SYSTEM BY BYPASSING THE SCHOOL AND BRINGING REAL LEARNING HOME.

Current Areas of Study

1) Guilford-Mecker structure & Mellot theory of mental abilities
2) left-right brain structure theory of learning pathways.
3) Computerized Delivery Systems
   MIT's logo
   Xerox's Smalltalk
   Hazeltine's Ticcit (MITRE) - (two way cable)
   CDC's PLATO
   Nat'l LIBRARY of Medicine's CAI Demo Lab.
   (PILOT LANGUAGE)

WRITER	DATE	WITNESS	DATE
JOE DECUIR	~~20 APRIL~~		

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

LIZA LOOP

REFERENCE: DAVID KAUFMAN
TOWARDS A
CYBERNETIC THEATER

CHILDREN WANT TO PUSH BUTTONS

Hey need them to learn about typewriters

~~LOOPS~~ HOW DO WE TAILOR
THIS TO WOMEN?
(SHE IS MORE INTERESTED IN PEOPLE)
ATARI CAN'T DO MUCH

Q: HOW SELF EXPLANATORY ARE THEY?

ANS: NOT - THAT'S WHY THEY FAIL.

LIZA THINKS WE SHOULD DELETE (OR MASK)
FEATURES SO THAT THE RESULT IS
LEARNABLE

'KEYBANGER' PROGRAMME FOR
PRELITERATES OR INCORRIGIBLES.

ONLY WANT TO CAUSE A RESPONSE.
(CAUSE AND EFFECT)

WRITER	DAVID KAUFMAN	DATE	20 APR 78	WITNESS		DATE	

GAME OR PROJECT

L2A LOOP

INITIAL PHASE FOR MANIPULATE MACHINE.

LATER, MACHINE INSTRUCTS.

'KEYBANGER' - PRACTICE CARTRIDGE.

MEASUREMENTS ON FLEX CABLES.

ADDRESS BUS DATA.

KIM 6502. LOADED BY KIM BOARD AND 8T97 BUFFERS WHICH IN TURN DRIVE DEVELOPMENT SYSTEM AND FLEX CABLES.

FLEX CABLES RECEIVED BY 7407'S.

no termination

7407 OUTPUTS w/ 1K(!?) PULLUPS.

8T97'S ~~HAD~~ HAD <10nsec rise time driving bus.

SWITCH WHEN 6502 RUNNING ~2VOLTS.

OF 8T97 { FALLING EDGES 110nsec AFTER ↓ Φ1
RISING EDGES 125nsec AFTER ↓ Φ1

10 nsec delay from 8T97 DRIVING CABLE TO 8T07 PULLING DOWN BB BUS. 2-3 nsec delay on cable.

WRITER JOSEPH DRUM	DATE ~~JOHN~~ 1/4/78	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
ANTIC CHANGES

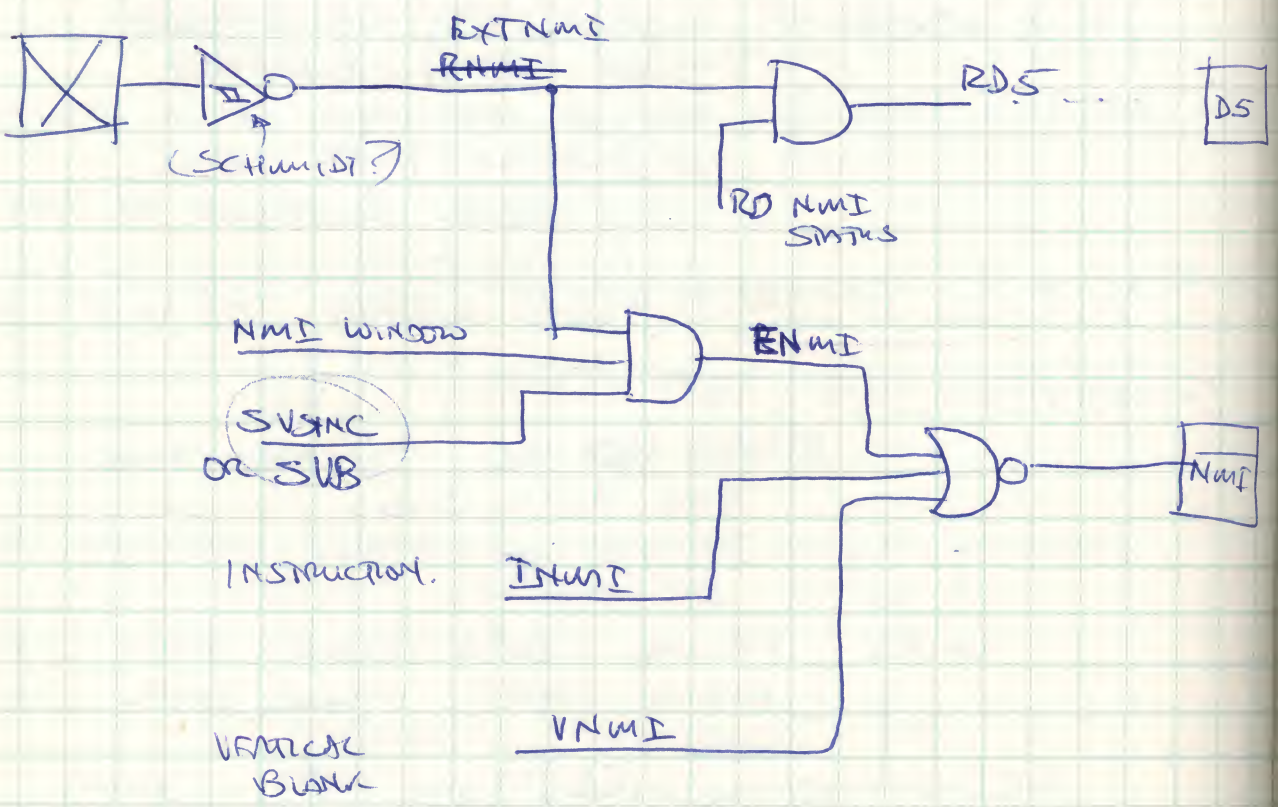
-to implement after breadboard comes back.

1). return VBLANK NMI to being maskable.

2) deleted CSYNC PIN.

3) Driving in external NMI PIN (RESET BUTTON) (SCHMIDT TRIGGER?)

4) STROBE IT WITH NMI WINDOW AND A LINE WITHIN VBLANK. LIKE SET VSYNC. READ OUT DATA BITS.



WRITER JOE DECUIR	DATE 29 MARCH	WITNESS	DATE

GAME OR PROJECT

COLLEEN.

UP TO DATE ADDRESS MAP FOR COLLEEN/CANDY

COLLEEN

F	PERSONALITY
E	MODULE
D	I/O
C	1ST CARTRIDGE
B	
A	2ND CARTRIDGE
9	
8	
7	16K RAM.
6	
5	
4	
3	16K RAM.
2	
1	
0	4K RAM

F/7	RESIDENT
E/6	O/S
D/5	I/O
C/4	1ST CARTRIDGE
B/3	
A/2	RAM EXPANSION.
9/1	
8/0	4K RAM

QUOTES ~~FROM~~ FROM ROY CASPAR
ON SYNERTEK

6551	25K	$5 each
	100K	4.50
6522	25K	4.50
	100K	400

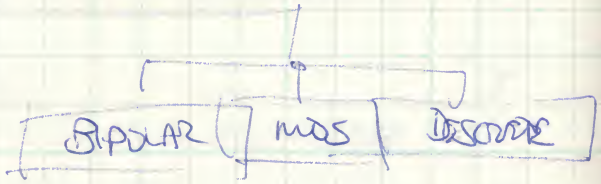
WRITER	DATE	WITNESS	DATE
JOE DECUIR	4 APRIL 78		

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
MOTOROLA 6847 DEMO.

ERNIE BARBARO. SALES.
DENNIS HAPGOOD APPLICATIONS ENGINEER
STAN KATZ MKTING MGR IN CONSUMER
JOE ROY (DESIGNER)
LE PROGRAM MANAGER, GAMES AND TOYS.

TED JARIS IS HEAD MARKETER
COMPUTER, FED
CONSUMER, AUTO, COMMUNICATIONS,
MKTING



- THEY ARE TRYING HARD TO [redacted]
DO COOPERATIVE DESIGN W/ AND FOR CUSTOMERS.

STRENGTHS - SEMI GRAPHICS COINCIDENT WITH CHARACTERS,

THIS IS DOING

1200, 600 FOR DISPLAY RAM (1K x 4S) (use ram)

THEY THINK EXTRA COST OF DYNAMICS IS HIGH,

PEL = PICTURE ELEMENT.

THEY USE BIPHASE SHIFT REGISTER TO GET HIGHER DOT RATE

WRITER JOE DECUIR	DATE 2/17	WITNESS	DATE

GAME OR PROJECT JOE ROY 602-244-3716

TRY DO EXTENDED INDIRECT ADDRESSING WITH EXTENDED PAGES NOW, WORKING ON A SEPARATE CHIP TO DO THAT.
32 POSSIBLE BYTES.

TRY PUT UP MULTICOLOR DEMO JUST LIKE ORIGINAL ATTIC DEMO.

"IF ~~GUYS CAME IN~~

"IF WE CAME IN WITH GOOD GAMES YOU GUYS WOULD FALL THROUGH" ROY

CHIP SET POINTED AT HOME COMPUTER
$30 for CHIP SET. (NOT COUNTING ROM)

6847 }
1372 }
6800 1MHZ ALL 5V.
6821
2 2114
7-12 74LS DRIVERS

18 CHIPS 78
5 CHIPS 79

TRY 'RACE THE BEAM' WHEN SCROLLING VERTICALLY.

GENERATE HARD RED AND BLUE BY PUMPING ~~RED~~ OUT 256×192 BITS IN ALTERNATING PATTERNS. CAN'T DISARM BURST

WRITER	JOSEPH DECUIR	DATE	WITNESS	DATE

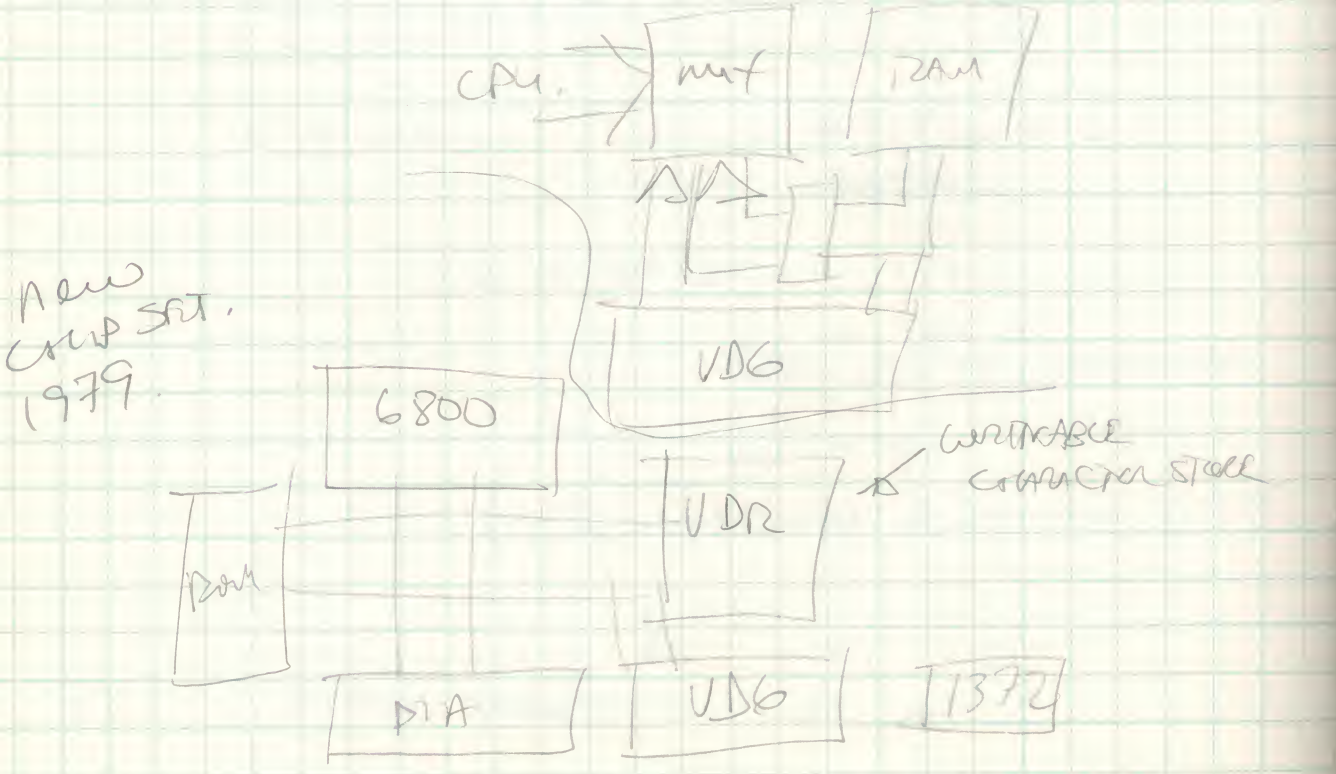
ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
VDG DEVICE FROM MOTOROLA

4 LUM LEVELS (INCL BLACK)
CORRESPONDS TO TMR COLORS

64×5×7 INTERNAL ROM,
(SEE PAGE IN 6847 WRITEUP)

2ND SYSTEM - 2 FUNCTIONS INTO RAM.
USING LATCHES AND MUXES.
(NEW CHIP WILL HAVE 1K×8 DYNAMIC RAM ON CHIP!?)
TO REPLACE



NEW CHIP SET.
1979

WRITER JOE DECUIR	DATE MAY	WITNESS	DATE

GAME OR PROJECT

VDG

UBIT PMF CAPABILITY.

SOFTWARE COUNTER
+ 8 INTERRUPTS.

ABSOLUTE MINIMUM

3870 + VDG + RAM.

~~6803 + VDG + RAM~~

~~68~~ 3870 + VDG + UDR + 1370

"DANGER OF OVERINTEGRATING"

WRITER	DATE	WITNESS	DATE
JOE DECUIR	1/27/83		

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
DOS 5¼

CURRENT TAPE FORMATS.

USE CUTS 2400/1200 BAUD.
TAPES

BAUD RATE 300 BAUD

SEE ADDA SPEC WRITTEN BY SIMONE FOR

~~AS~~ NEW FEATURES.

VARY CHARACTER SIZE

" CHARACTER SET

" CURSOR MOVE

[redacted]

MEMORY MAP MODES

SPECIAL GRAPICS FIELD (W/ OBJECTS)

JAY MAKES POINT THAT

A VERSATILE CONTROL CHARACTER SET ~~IS~~ WILL

ALLOW ALL PARTS OF MACHINE

TO BE USED EVENTUALLY.

WRITER [illegible] DATE 3 MAY 78 WITNESS DATE

GAME OR PROJECT
DORSETT.

(HE'S GOING TO TRY TO DO CAI WITH A TRS-80)
TRYING TO ADD AUDIO TO IT.

CHECK ANTIC VIDEO CODE LOGIC.

BLANK - TURN INVERT.
RATHER THAN INVERT, AND BLANK

THIS BIG QUESTION. ARE ALL THE BELLS AND WHISTLES NECESSARY? (OR SUFFICIENT)

IDEA. USE UNUSED LINES IN TEXT FIELD (OR PSEUDO LINES IN THE DISPLAY SPACE) AS LOCATIONS OF CONTROL 'REGISTERS'.

WRITER DE DORSETT	DATE 5 MAY	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
Colleen Development System

EVALUATION / CHARACTERIZATION OF

BUS INTERFACE

ADDRESS LINES
Z2 → BB

~~UNLOADED~~
6502 OUTPUT
TO BB BACKPLANE

↑ = RISING EDGE TO RISING EDGE @ 2V.
↓ = FALLING EDGE TO FALLING EDGE @ 2V.

AΦ	Z2 → BB	↑ 22nsec.	↓ 36nsec.

CLOCK DELAYS

Φ_0 OUT	↑	TO Φ_2 IN	↑ 112nsec
Φ_0 OUT	↓	TO Φ_2 IN	↓ 100nsec

31 MAY 78

WRITER	DATE	WITNESS	DATE

ATARI **ENGINEERING LOG SHEET** 81

GAME OR PROJECT
COLECO SYSTEM.

AFTER SPENDING THE MONTH OF JUNE DEBUGGING THE FIRST DEVELOPMENT SYSTEM...

SCHEMATICS:
- CLOCKING CKTS.
- KEYBOARDS.
- COLECO
- CPU BOARD
- RAM BOARD

DON'T EXIST.
- CANDY
- PM
- CARTRIDGES.
- OTHER BOARDS IN BOX.

TIMING DIAGRAMS.
- RAM TIMING
- CLOCKS
- SYSTEM TIMING DIAGRAM.

SPECS.
- CHIP PINS. INFO COLECO MANUAL.
- SYSTEM TIMING
- I/O PORTS.

DRAWINGS.
- KEYBOARD LAYOUT.
- ASSORTED MECHANICAL.

WRITER	DATE	WITNESS	DATE
DECUIR	6 JULY 78		

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
COUPE SYSTEM.

CHANGES

1. RAM CARDS. SEE ANNOTATED PRINT.

   NILES GROUP RESPONSIBLE FOR RAM CARDS, CHECK ON JUMPERS ON MUX MAT.

2. CHECK RAM TIMING
   ~~RADIS~~ W/ REGARD TO REAL BOARDS
   W/ REGARD TO REST OF SYSTEM.

3. REWIND CLOCK TIMING
   W/ RESPECT TO SYSTEM.

4. PIA ADDRESSES.
   REVERSE ADDRESS LINES
   AS PER MANUAL.

5. SERIAL PORT CHANGES,
   ~~AS PER~~
   SIRQA, SD,
   SIRQB, SCLKS
   M60 ETC.
   GND.

6. CHECK PULLUPS AS PER
   CHIP PINOUTS IN MANUAL.

7. ADDRESS MAP.
   AS PER MANUAL.

8. RESET BUTTON.

9. ~~LOUT~~ TIA 53 DRIVES
   LOUDSPEAKER VLA XPNSTORS.

WRITER	DATE	WITNESS	DATE
DAVE			

GAME OR PROJECT
COMPOSITE SYSTEM CHANGES.

10. UP DATE LIGHT PEN STUFF

11. DIRECT VIDEO ?

12. ~~STILE HAUS TEST CONNECTOR (A~~ ~~OR~~
TEST CONNECTOR FOR CANDY, KEYFOB ?.

13. ADD NOTES : ASSIGN MEET OF TIA LINES,
WHICH LINES GO TO SERIAL PORT.
8304 OS LS 245

14. PULL SYNC OF CPU BOARD CONNECTOR.

15. UP DATE LSI PINOUT CHANGES OF
650X, ANTIC. CTIA

16. UP DATE NOMEN CLATURE.

17. CANDY : PM. ?
RAM EXPANSION ?
SERIAL PORT ?

18. RAM CARD CHANGES

WRITER	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
Colleen O.S. "COS"?

INTERRUPT HANDLERS.
MODULE INTERFACING
RESOURCE ALLOCATION
I/O PROTOCOL
DEVICE DRIVERS.
ANTIC DRIVERS.
KEYBOARD DRIVERS
GENERAL UTILITIES
MONITOR COMMANDS.
SYSTEM EXPANSION
COLLEEN VS CANDY
DOSSET

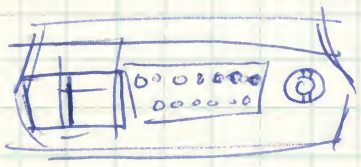
RAM
ZP
CHIP I/O
PLAYFIELD
PLAYFILE
SERIAL PORT
KEYBOARD
AUDIO
CONTROLLERS.

DYNAMIC MEMORY ALLOCATIONS.
ZP/STACK
REST OF RAM.

CANDY.:

{ 4 GAN D'S.

SIDE POWER JACK
13 PIN D CASSETTE
RF CABLE.
CH 3 4 ON BACK.
POWER ON/OF ROCKER.



1	V
2	R
3	Q
4	I
5	N
6	N
7	S
8	V
9	A
10	A
11	A
12	A
13	A
14	A
15	A
16	A
17	A
18	A
19	A
20	A

WRITER | DATE | WITNESS | DATE

GAME OR PROJECT

COLLEEN SYSTEM.

COLLEEN/CANDY PART NUMBERS. (LSI)

CPU C012297-BA
ANTIC C012296-BA
CTIA C012295-BA
POKEY C012294-BA
PIA C012298-BA

4K RAM C012295-BA
16K RAM C012969-BA

16K ROM C0123XX-BA
32K ROM C0124XX-BA

INSERT IN SCHEMATICS.

-01	AMI	-10	AMD
-02	EA	-11	MIC
-03	SYNERTEK	-12	ROCKWELL
-04	MTI	-13	WESTERN DIG.
-05	MOTOROLA	-14	ADV. LSI. TECH
-06	MOS	-15	NEC
-07	GI	-16	SPI
-08	S16	-17	SUPERTEX
-09	MOSTEK	-18	TI

PIN #'S.

CPU		ANTIC		CTIA		POKEY		PIA		
VSS	RES	VSS	D7	A1	A2	VSS	D2	VSS	CA1	26
RDY	Φ2	LP	D6	AΦ	A3	D3	D1	PAΦ	CA2	39
Φ1	S.O.	AN2	D5	VSS	A4	D4	DΦ	PA1	IRQA	38
IRQ	R/W Φ0	AN1	D4	D3	D4	D5	AUD	PA2	IRQB	37
NC.	HALT	ANΦ	RES	D2	D5	D6	AΦ	PA3	RSΦ	36
NMI	nc	RNMI	FΦ0	D1	D6	D7	A1	PA4	RS1	35
SYNC	R/W	NMI	Φ0	DΦ	D7	Φ2	A2	PA5	RES	34
VCC	DBΦ	HALT	D3	TΦ	R/W	P7	A3	PA6	DΦ	33
AΦ	D1	REF	D2	T1	CS1	P6	R/W	PA7	D1	32
A1	D2	A3	D1	T2	CSΦ	P5	CS1	PBΦ	D2	31
A2	D3	A2	DΦ	T3	Φ2	P4	CSΦ	PB1	D3	30
A3	D4	A1	A4	SD	FΦ0	P3	IRQ	PB2	D4	29
A4	D5	AΦ	A5	S1	OSC	P2	SOD	PB3	D5	28
A5	D6	R/W	A6	S2	VDD	P1	CLK	PB4	D6	27
A6	D7	RDY	A7	S3	HALT	PΦ	BCLK	PB5	D7	26
A7	AB15	A10	A8	DEL	CSYNC	KR2	KR1	PB6	Φ2	25
A8	A14	A11	A9	COL	LΦ	VDD	SIO	PB7	CS1	24
A9	A13	A12	A15	PAL	L1	K5	KΦ	CB1	CS2	23
A10	A12	A13	A14	ANΦ	L2	K4	K1	CB2	CSΦ	22
A11	VSS	Φ2	VDD	AN1	AN2	K3	K2	VCC	R/W	21

WRITER	DATE	WITNESS	DATE
DECKER			

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
X-Y JOYSTICKS

WADE, DAVE, JERRY, CRAIG, ROY, JOE

TWO PROBLEMS FROM OUR END,

1) CHANGE CAPACITOR SIZE OR
ADJUST POT VALUES
TO KEEP IT CENTERABLE

2) WHAT DO WE GET ENOUGH
PROTOS FOR PROGRAMMING
PURPOSES.

NOTE, I NEED TO CALIBRATE
THE HAT VALUES FROM
POKEY

TEST PROCEDURE THAT MOVES A
PLAYER AROUND. - AUTO ZEROING ON RESET.
- ADJUST TO 60° or 90° POTS.
AVERAGING, NOT AVERAGING

CAPACITORS ±5%
SAMPLE BOTH POTS @ 1 LINE.
MOVE CURSOR AND DISPLAY VALUES.
OPTIONS, 60°, 90°
USE 2ND SET OF ORDINARY
POTS FOR OFFSET.?

MULTIPLY, DIVIDE BY
× ½, × 1, × 1½, × 2
WITH, WITHOUT 2 FRAME FILTERING.
EQUIPMARKS, HASH MARKS.

WRITER DECUIR	DATE 10JUL78	WITNESS	DATE

GAME OR PROJECT
COLLEEN / CANDY

COUNTING INTERCONNECT AMONG BOARDS.

MOTHER BOARD:

→	CONTROLS 1-4	9 PIN 'D'		4
→	CPU BOARD	56 PIN	EDGE	5
→	PM	44 PIN	EDGE	6
→	RAM 1	44 PIN	EDGE	7
* →	RAM 2	44 PIN	EDGE	8
* →	RAM 3	44 PIN	EDGE	9
→	CART 1	24 PIN	EDGE	10
* →	CART 2	24 PIN	EDGE	11
→	KEYBOARD	18 PIN	FLEX	12
→	AUX?			13

AUX?
- S0
- S1
- S2
} PANEL

(S3 BUFFER) NOT ON KEYBOARD?

- NMI } PANEL
- COMP VIDEO } MODULATOR
- COMP VID - CHROMA } DIN JACK
- ~~GND~~ CHROMA
- AUDIO OUT
- AUDIO IN
- $\overline{\text{SIRQA}}$
- $\overline{\text{SIRQB}}$
- $\overline{\text{M6D}}$
- $\overline{\text{CMD}}$
- SOD
- SID
- OCLK
- ~~BCLK~~
- VBB
- VSS (2)
- VCC (2)
- VDD

SERIAL PORT

23+ LINES

POWER

VB+?

WRITER	DATE	WITNESS	DATE
JOE DECUIR	15 JUL 78		

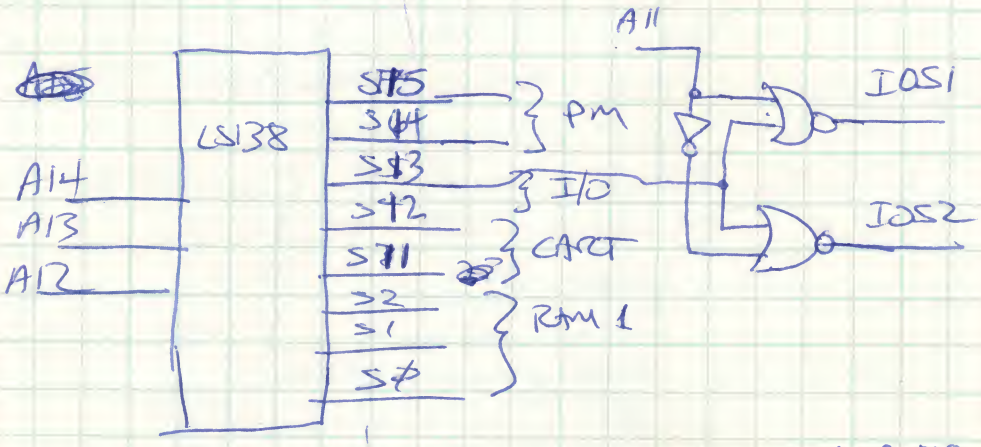
ATARI ENGINEERING LOG SHEET

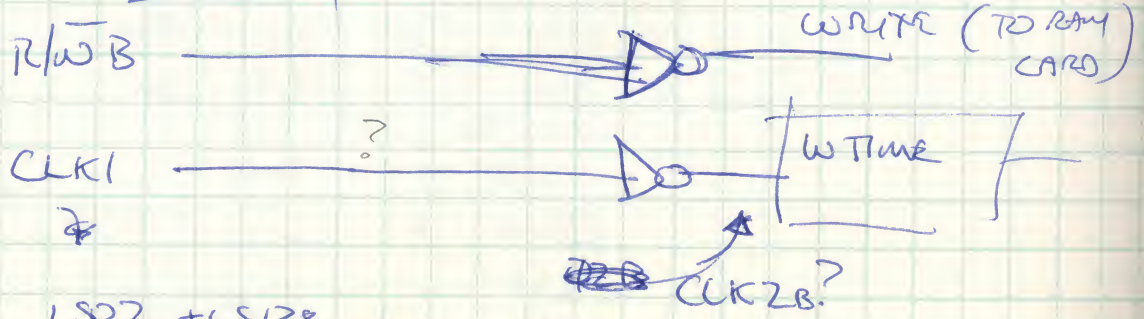
GAME OR PROJECT

CONNECTIONS TO BOT, CANDY, COLLISN

COLLISN	CANDY
9VAC	9VAC
RFOUT	RFOUT
DIN OUT	X
SERIAL PORT	SERIAL PORT
CONTROL 1	CONTROL 1
2	2
3	3
4	4
CART 1	CART 1
CART 2	X
RAMS, PM	X

CANDY SSI/MSI





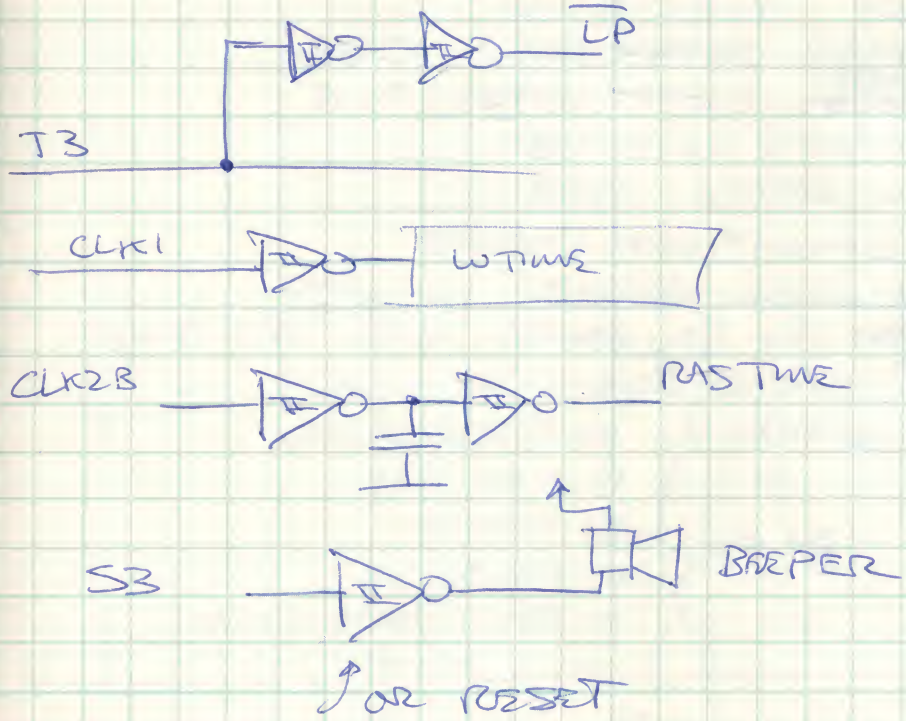
LS02 + LS138
+ LS04? + 2 LS244 on CPU CARD
+ RAM CARD STUFF

WRITER	DECKER	DATE 10 Sept	WITNESS	DATE

GAME OR PROJECT
COLLEEN/CANDY SSI/MSI

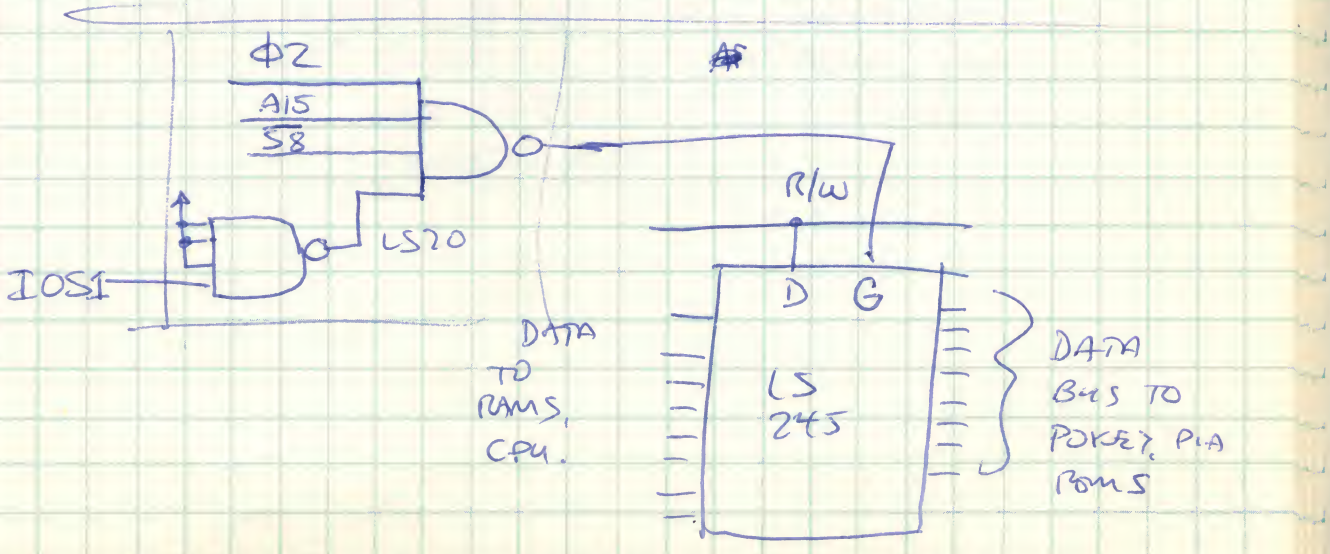
ALTERNATIVE

USE 3RD PART LS14



ADD TO COLLEEN. LS138, LS245, LS20

- 2ND LS138 ~~S5~~ S3, 4, 5, 6, 7, 8, 9, 10



WRITER	DATE	WITNESS	DATE
DECUIR	10 Jan 4		

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

COLLEEN / CANDY

PRINTS NEEDED.

#2 D+E
#1 D
#6 C
#7 C
#3 C+D
#5 C
#4 C
#8 C

#1 COLLEEN MOTHERBOARD
#2 CANDY MOTHERBOARD
#7 COLLEEN SUPPORT BOARD SIDE
#8 CANDY SUPPORT BOARD SIDE
3 CPU/ANTIC/TIA BOARD
4 RAM 4K/16 BOARD
5 PERSONALITY MODULE BOARD
6 CARTRIDGE BOARD
2716 PM BOARD, 2716 CART BOARD
#10 CONTROLLERS: A X-Y
#9 KEYBOARD
B KEYBOARD
C LIGHTPEN
D JOYSTICK
E POTS
F DRIVING CONTROL.

BY I/D

BY ID

COLLEEN
CANDY
CPU
RAM
ROMS
COLLEEN SUPPORT
CANDY SUPPORT
KEYBOARD

WRITER	DEANER	DATE	11 JULY 78	WITNESS		DATE	

GAME OR PROJECT

CANDY / COLLEEN PATENT MEETING

	TOPIC	INVENTOR
1.	SERIAL ~~BUS~~ PROTOCOL	SCOTT
	"	
	"	
2.	AUDIO ~~POLY COUNTER AS NOISE GENE~~	DAVE
	SAMPLED POLY COUNTER	
	___ LOOKS LIKE 4	
	LOW PASS FILTER	
	COLOR HIGH PASS FILTER	
3.	PRIORITY ENCODING CKTS ? (ALSO ON STELLA)	GEORGE
~~6~~	COLLISION CKTS.	
4.	ANTIC DISPLAY COMPUTER (OVERLAPS w/ SERIAL OTHER DEVICES) } ETC. SEGMENT SCREEN MODES.	ANYTHING SHOWN MUST BE PATENTED IN THE YEAR
5.	COLOR SYSTEM?	STEVE
6.	ANTIC INSTRUCTION SET.	JOE
7.	PLAYER MISSLE DMA.	STEVE ~~JOE~~
8.	FOUR COLOR STAMP MODE.	~~STEVE~~ STEVE
9.	DEFENDERS	JOE
10.	SCROLLING	V SCROLLING & JOE AND ZONES & FRANCOIS.
11.	H SCROLLING	
~~12~~ 12.	MICROPROCESSOR HALT	JAY
13	PAL COLOR DELAY LINE (KEEP QUIET TELEFUNKEN HAS PATENT ON PAL COLOR MODULATION)	JAY

WRITER	DATE	WITNESS	DATE
DECUIR	11 JULY 78		

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
COUSRY DOCUMENTATION.

NILES, DO YOU NEED COLOR ADJUST ON CPU CARD

NILES WANTS ADDRESS MAP,

POWER REQUIREMENTS OF NEW LSI.

POWER ON 4K ROMS,
LINE LIMIT TO BE 100MCS.

NILES WANTS TO MOVE CHIP TO PROCESSOR

CANDY'S ROM IS ON MOTHER BOARD. NO PM.

LOOK INTO OTHER ONE CHIP DECODING FOR CANDY.

REVISED REFRESH TIMING FROM ANTIC.

ON CANDY SWITCHES. NMI

LOOK AT CAPACITIVE LOADING,

WHAT HAPPENS IF BUFFERING IS CHANGED SO THAT OUTPUTS OF ROM GO THRU UNIDIRECTIONAL BUFFERS OUT PAD OF LS245

WRITER	DATE	WITNESS	DATE

GAME OR PROJECT

RAMS, 20-25 pF / DATA BUS PIN.

LOOKING NEED FOR 1.8K ?

CAN THEY BE BETWEEN

CHIP AND CAPACITORS.

GET RB SCHEMATIC ~~TO~~

FOR CANDY FROM ATARI

PANELS SWITCHES GO ON KEYBOARD
CONNECTOR IN CANDY

CONNECT-WIRE TO BD2.

~~DRILL~~ LEAVE ON CONNECTOR,

BRING TO OF THE CARD.

JAY WANTS AN ANALYSIS TO
VERIFY THAT THE PROPOSED UNIDIRECTIONAL
BUFFER SCHEME FOR CANDY DOES
NOT CAUSE ANY TROUBLE, PARTICULARLY
ON SKEW BETWEEN DATA AND CLOCK ON WRITES.

WRITER	DECUIR	DATE	13JUL78	WITNESS		DATE	

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
COLLEEN, PERSONALITY MODULE

USE of AM9511 APU
'ARITHMETIC PROCESSING UNIT'

— GREAT DEAL of TROUBLE,

IT LIKES TO YANK on RDY for
EXTENDED PERIODS. - ≥ 560nsec

WRITER | DATE | WITNESS | DATE

GAME OR PROJECT

DUMB CASSETTE FREQUENCIES

SPECS

600 BAUD from CH3, CH4 together.

CH1 LOGIC 1 = 5326 Hz = 8*665.8Hz

CH2 LOGIC 0 = 3995 Hz = 6*665.8Hz

RUNNING CH1 AND CH2 off 64kHz 63.9204

$$FOUT = \frac{FIN}{2(AUDF+1)}$$

$\frac{3.58 mHz/2/28}{5326 = 6 = 5+1}$

$3995 = 8 = 7+1$

RUNNING CH3 & CH4 together off 1.79 mHz

$$FOUT = \frac{FIN}{2(AUDF+7)} \quad \left(\frac{FIN}{2(AUDF+4)} \text{ IF CH4 ONLY}\right)$$

1491.47 .00032 ERROR

$$(AUDF_{CH1}+1) = \frac{3.579575 mHz/2/28}{2(5326)} = 6 \qquad AUDF_{CH1} = 5$$

$$(AUDF_{CH2}+1) = \frac{3.5795+5mHz/2/28}{2(5326)} = 8 \qquad AUDF_{CH2} = 7$$

$$AUDF_{CH34}+7 = \frac{3.579555/2}{2(600)} = 1491.47 \qquad AUDF_{CH34} = 1484$$

WRITER	DECUIR	DATE 23Aug78	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

GALLUP STUDY PERSONAL COMPUTERS

774 men, 762 women 18+ YRS DONE JAN 78

PRINCIPAL FINDINGS

CONSUMER AWARENESS of COMPUTERS for HOME IS LIMITED 32%

RELATIVELY FEW REPORT ANY FIRST HAND EXPOSURE (32%)

THOSE AWARE ARE KNOWLEDGEABLE 41% PERSONAL FINANCE

27% RUN HOUSE, 27% KITCHEN, 14% EDUCATION

25% INTERESTED IN GENERAL CONCEPT

'VERY STRONG' INTEREST <35 YRS 14%, COLLEGE 18%,

>$20K/YR 14%, PROFESSIONAL AND BUSINESS 16%

51% of COMPUTER JOCKS, 19% of EVERYBODY ELSE

EDUCATION AND HOUSE CONTROL MOST ~~INTERESTING~~ INTERESTING

KITCHEN AND GAMES LESS INTERESTING

INTEREST IN CONTROL FUNCTIONS HIGHER IN WOMEN, BLUE COLLAR, LESS EDUCATED

EDUCATION PROGRAMS HIGH IN CONSUMER APPEAL - BUT

PEOPLE EXAGGERATE THAT INTEREST

FINANCE AND CLERICAL ~~NOT~~ INTERESTING, BUT ARE APPEALING

GAME PROGRAMS DO NOT STIMULATE MUCH INTEREST

INTEREST IN PROGRAMS NOT STRICTLY RELATED TO NEEDS

BUT RATHER AVAILABILITY SUGGESTS UTILITY.

32% of ACCEPTORS WANT TO PROGRAM BADLY, 37% SORT OF, 22% LITTLE

SELF PROGRAMMED 57 AND PRE PROGRAMMED 32 BOTH INTERESTING, (BOTH 18)

YOUNG AND WEALTHY WANT SELF PROGRAMMING

COMPUTER JOCKS WANT TO PROGRAM, OTHERS PREPROGRAMMED.

MOST INTENSELY INTEREST - MOST DESIRE TO PROGRAM.

AMONG GENERAL ACCEPTORS 2:1 FINANCE AND EDUCATION/VS GAMES + KITCHEN

CONSUMERS UNDERESTIMATE CASSETTE ~~COST~~ PRICES UNDER 4:1 MEDIAN $25

21% of EVERYONE HAS SOME INTEREST IN BUYING ONE

92% of EVERYONE ~~.~~ STRONG INTEREST

APPEALS TO NEW, YOUNG, WELL OFF

WEST COAST HIGHEST INTEREST, COMPUTER JOCKS

LIKELY BUYERS, YOUNG, WELL OFF, COMPUTER JOCKS

HIGHER AMONG OWNERS OF OTHER ELECTRONIC APPLIANCES

	PROGRAM	PRE PROGRAMMED	BOTH
COMPUTER JOCKS	51	22	22
NO KNOWLEDGE	28	33	18

WRITER	DATE	WITNESS	DATE

GAME OR PROJECT

GALLUP STUDY (CONT)

PRICE EXPECTATIONS ~~$1000~~ <500 26%, >1500 23% MAD ~1000

SOONEST, AVERAGE >1000

$600 ONLY SLIGHTLY MORE INTERESTING THAN $1000 18% VS 14%

20% @ $300

22% THINK PRICES WILL FALL A LOT, 41% SOMEWHAT

IBM AND XEROX INSPIRE CONFIDENCE

ALSO SONY, TI, AND RCA

23% EXPECT TO BUY FROM SPECIALTY STORE

AVAILIBILITY of SERVICE DEPARTMENT VERY IMPORTANT 67%

TECHNICAL ADVICE 60%

CASSETTE AVAILIBILITY 44%

CLASSROOM INSTRUCTION 35%

PEOPLE ~~WHO~~ ~~WHO~~ HAVE TROUBLE WITH:

EXPRESS INTERESTS IN COMPUTERS ARE SOMEWHAT MORE LIKELY TO EXPRESS INTEREST IN HOME COMPUTERS

~~LIVING BUFFS~~

	EVERYBODY				
16 TASKS	10	9,8,7	6,5,4	3,2,1	0
ALARMS	62	22	7	7	2
EDUCATION MATH LANGUAGES WRITING	46	29	13	10	2
CONTROL HEATING, AC	44	30	10	15	1
AUTO MAINTENANCE REFERENCE	44	29	12	13	2
SMALL APPLIANCES	35	32	15	16	2
CHECKBOOK BUDGETING	38	29	16	15	2
PERSONAL CALENDAR	42	23	10	21	4
FOOD INVENTORY	28	27	19	25	1
APPT CALENDAR	26	28	24	21	1
MAILING LISTS	25	28	24	21	2
CONTROL KITCHEN	26	25	23	24	2
BOARD, CARD, STRATEGY GAMES	20	25	30	23	2
CALC. CALORIES	17	25	23	32	3
FAST ACTION GAMES	16	21	20	36	1
RECIPES	10	19	28	34	3
SPORTS STATISTICS	14	18	22	44	2

future OTHER USES/FEATURES

VERBAL INSTRUCTION

VERBAL RESPONSE

BUILT INTO TV

UNLOCK DOORS VERBALLY

SHOP FROM HOME

ROOM BY ROOM TEMP CTRL

ELECTRONIC MUSIC

PRINTER

TALK TO OTHER COMPUTERS

WRITER DECKER | DATE | WITNESS | DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

SURVEY (CONT)

FUNNY BODY

ATTITUDES TOWARD MERS:

(DEGREE OF CONFIDENCE)

(AMONG PRODUCT ACCEPTORS)

	10	9-7	6-4	3-0	?	never heard of	10	9-7	6-4	3-0	?	never heard of
IBM	49	29	6	+	7	9	49	31	6	1	9	4
XEROX	42	37	6	1	5	9	43	41	5	0	6	5
TI	29	39	7	2	6	17	29	45	5	2	7	12
SONY	26	47	10	3	4	10	26	56	8	2	5	4
RCA	20	46	18	2	6	8	17	55	17	3	6	2
RADIO SHACK	10	31	30	12	8	9	9	35	30	13	10	3
HP	10	16	9	5	8	52	14	17	8	7	8	46
SEARS	9	36	30	9	6	10	8	42	32	9	6	3
LAFAYETTE	6	22	21	7	8	36	6	28	21	7	7	31
PARKER BROS	5	17	29	19	11	19	7	19	31	20	12	11
MILTON BRADLEY	5	16	28	22	11	18	5	17	31	21	13	13
MATTEL	5	16	21	24	12	22	6	20	22	22	14	14
HITACHI	4	25	20	6	13	32	4	30	23	6	14	23
HEATH	4	14	14	7	9	52	4	18	13	7	13	45
ATARI	2	11	9	7	10	61 !	2	14	8	7	15	54
COMMODORE	1	4	9	9	8	69	1	3	7	9	11	69
APPLE	(NOT INCLUDED)											

↑ PRESENTED ALPHABETICALLY.

ATARI $\frac{2\times10+11\times8+5\times9+2\times7}{29} = 5.7$

IBM $\frac{49\times10+8\times29+6\times5}{49+29+6\ 87} = 8.9$!!

SEARS $\frac{9\times10+36\times8+30\times5+9\times2}{84} = 6.5$

TI $\frac{29\times10+39\times8+7\times5+2\times2}{77} = 8.3$

RADIO SHACK $\frac{10\times10+31\times8+30\times5+12\times2}{83} = 6.2$

LIKELY BUYERS

WE EXPECT TO BUY SOON FROM SEARS OR RADIO SHACK!!

GAME OR PROJECT

SURVEY (CONT)

WOMEN REGARD HANDHOLDING (SALES PEOPLE) MORE IMPORTANT
WOMEN MORE INTERESTED IN PRE PROGRAMMING
WOMEN MORE INTERESTED IN PRE PROGRAMMED
WOMEN MORE INTERESTED IN CLASS ROOM INSTRUCTION

STRANGELY, DESPITE ~~LOSS~~ RELATIVELY LOW INTEREST IN 'GAMES' MOST EVERYBODY BELIEVES THEY SHOULD BE FUN.

WRITER	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
NOTES ON ODESSEY 2 DISSECTION

USES 2 9 PIN D CONNECTORS
FOR CONTROLS, UNKNOWN PINOUT

LSI INARDS:

8048 CPU. (64 BYTES OF RAM)

28 pin "8244" INTEL CUSTOM
PROBABLY VIDEO CHIP

24 PIN "SCM 67205P"
MOTOROLA PART

SMALL RESISTOR NETWORK.
2(74C175'S) - near keyboard

1 '612230-1' MOTOROLA PART

MAGNAVOX PART II

1 74LS148 PRIORITY ENCODER
1 74LS32
1 74LS00
1 "(612160-3")" from EXAR

30 PIN CARTRIDGE CONNECTOR

MISCELLANEOUS I/O PARTS
UNDER SHIELD

16 PIN FLEX TO KEYBOARD

GAME OR PROJECT

GENERAL PURPOSE INTERFACE

1) STEVE'S PROPOSAL ~$100 retail

CHEAP BOX 6502/1 w 5 3448A DRIVERS.

<9600 BAUD RS232
16 PARALLEL
02 TALKER/LISTENER 488
+ 2 3AMP AC RELAYS.

---

2) 4 JOE'S INTELLIGENT PRODUCT ~$150

6504 + 2316 + 6532
+ 3 × 6551
3 HIGH PERFORMANCE RS232

2B) REPLACE 2 6551's BY
68488 + 4 × 3448A

3) GENERAL PURPOSE I/O INTERFACE

6502 + 6532 + 2×2114 + ANTI POKEY
4 GENERAL PURPOSE SLOTS.

4 TYPES of I/O DEVICES:
RS232 (6551)
GPIB (68488 + 4 × 3448A + SWITCHES)
16 LINE DIGITAL (6520 + BUFFERS)
16 CHANNEL ADC (MUX + DAC + PIA)

WRITER	DECUIR	DATE 16 FEB 82	WITNESS	DATE

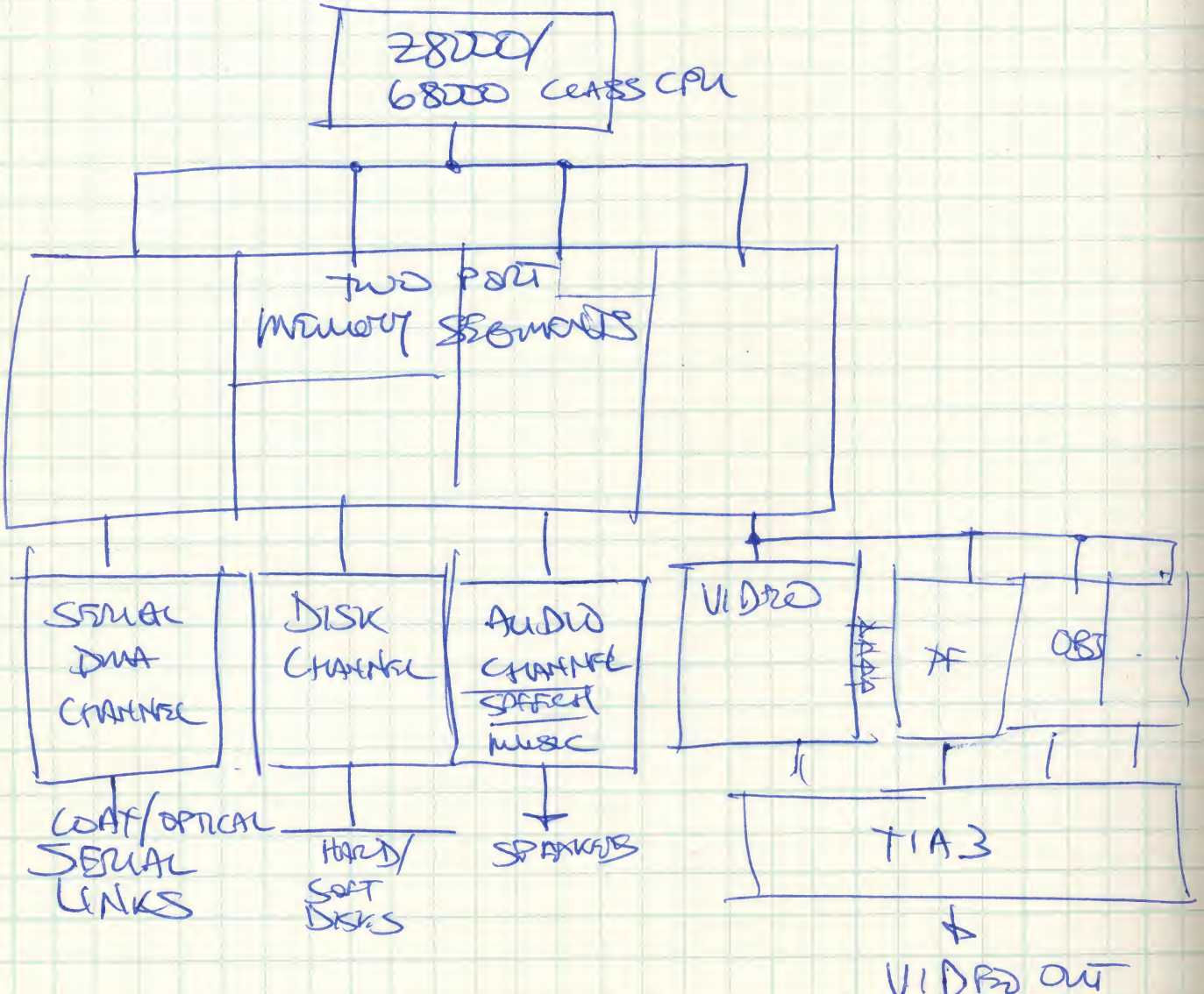
ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

12.096 XTAL 90-102 ATARI PART #

PROPOSAL FOR 'STOPS OUT'

HIGH POWER ENTERTAINMENT COMPUTER



8/11

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RAINS	2799
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