LABORATORY NOTEBOOK

In Custody of

Jack Kilby

Date of Issue

June 12, 1958

Property of

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TEXAS INSTRUMENTS
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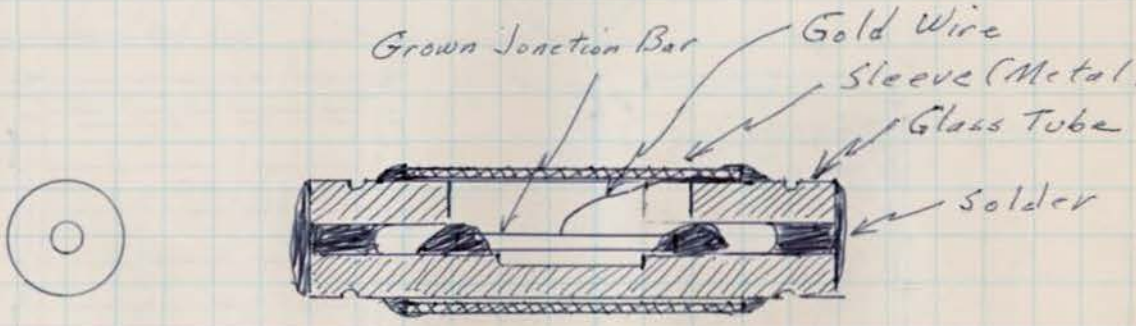
DALLAS, TEXAS

EO NO. 043C01
DATE June 13, 1958

Method for Assembly of Circuit Elements.

Many electrical circuit elements can be most economically manufactured in a rod or tubular form. This form has many advantages in processing and material handling. Resistors and tubular capacitors are currently available. Transistors could also be made in this shape, as shown by the sketch below.



Such a transistor could be assembled with no operations not now required for assembly to headers. A routing for this unit would be:

1. Cut glass or ceramic tube to length
2. Metallize all surfaces
3. Grind shallow notch in ends
4. Grind deep notch in center
5. Solder junction bar in place
6. Etch
7. Gold bond
8. Etch & gold plate
9. Clean
10. Slide metal sleeve in place
11. Solder dip ends to seal

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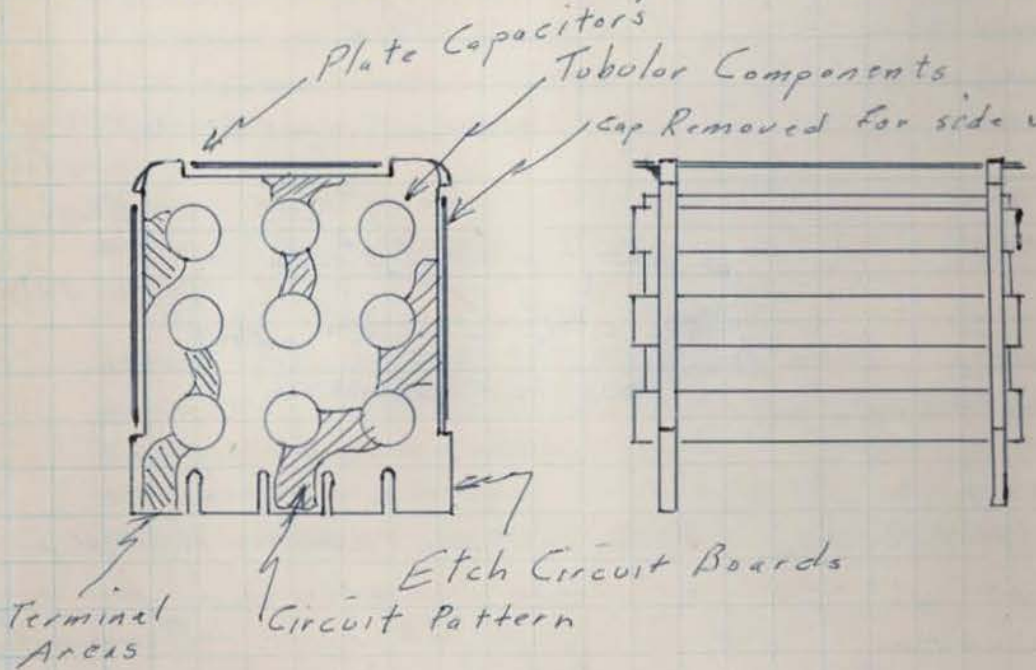
DATE June 13, 1938

A model of this transistor, about five times actual size, has been constructed at my request by H.N. Riser. This unit is now complete. Brass tubing for the sleeve and glass tubing has been ordered for the construction of working models.

Such transistors could be readily assembled with other tubular components as shown below:

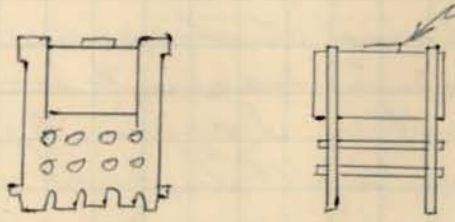


Up to nine tubular components could be dropped into place, by machine if desired. Since large values of capacitance can best be obtained in plate form, they have been used on the side & top of the unit. The connections between components would be made by conductors on the etched circuit boards. One end of each board has been shaped to serve as a lead — that is, the terminal

EO NO. 043601
DATE June 13, 19

areas could be dropped thru a slot in a mother circuit board. Connection between the component and the board would be made by dip or flow soldering. The entire unit could be potted if desired. This unit could be made small enough to go into a 3/8" cube, although this should not be the most economical size for the components.

A large component, such as an IF transformer, could be fitted in between the etched circuit boards as shown:



A very rough model of this unit, 5 time size, was completed May 23, 1958 and shown to Willis Adcock, Mark Shepard, Charles Phipps, and others.

To test the feasibility of the idea, an IF for a portable radio will be constructed.

J. S. Kilby
June 13, 1958

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EO NO. 043601

DATE ~~June~~ June 27, 1958

The first working model of the transistor shown on page 1 was completed today. The tubes used were metallized with gold paint by H N Rice, and the junction was assembled by Phil Trgovac. The gold metalizing does not tin readily, and the unit is probably not hermetically sealed.

J S Kilby
June 27, 1958

Five more good transistors meeting the 2N308 + 2N309 electrical test spec were completed on July 3. These units used Hanovia silver paint, and appear to be well sealed. They will be used to construct an IF Strip.

J S Kilby
July 3, 1958

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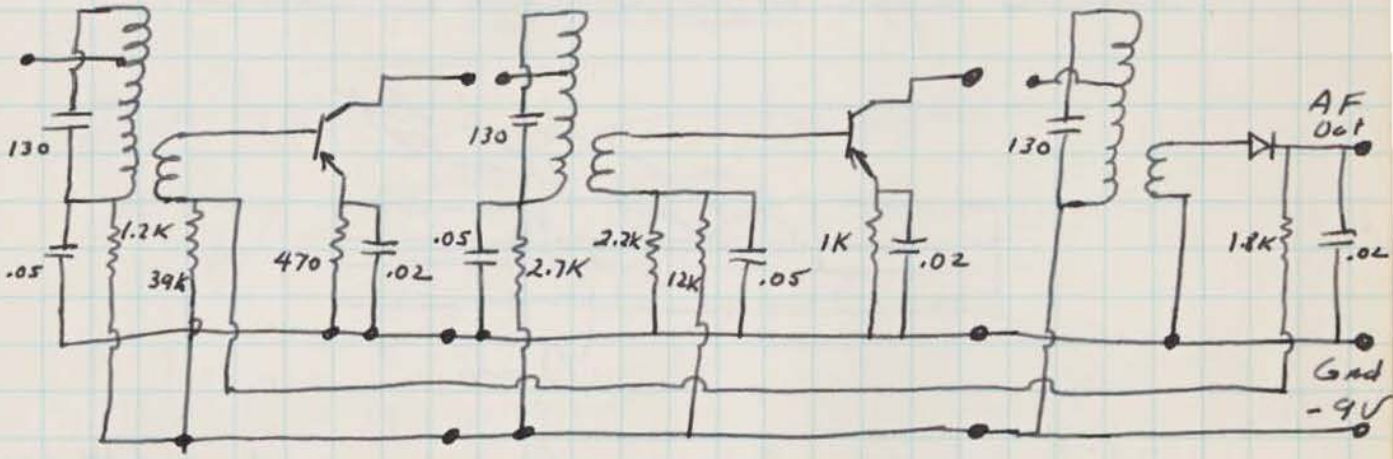
DATE July 12, 1958

A complete IF strip, consisting of two stages of amplification and a third stage with a diode detector has been constructed with the circuit below.



This circuit was developed by Rodger Weber. The three stage, when constructed, were assembled on a small mother board for testing. After correcting an error in the second stage, the unit was found to have 54 DB electrical gain. This test was witnessed by Rodger Weber.

J. S. Kirby
July 12, 1958.

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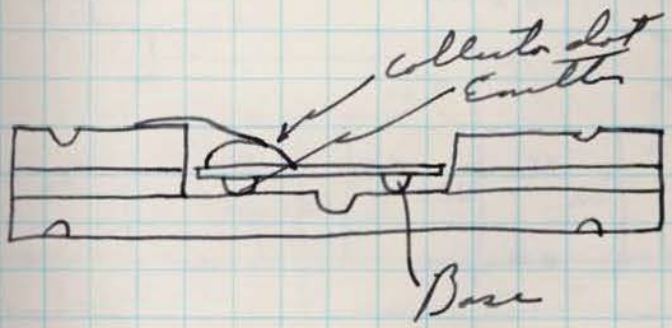
DATE July 13, 1958

The three IF stages were assembled into a small radio chassis originally made for Philco + demonstrated to Willis Adcock, Charles Phipps, Mark Shepard, and others. Detail drawings of the parts used in this set are being made.

Alloy transistors can be made in the same type of enclosure as shown:



This construction is shown in dwg JLK 601-2 ~~of this date~~ of July 11, 1958.

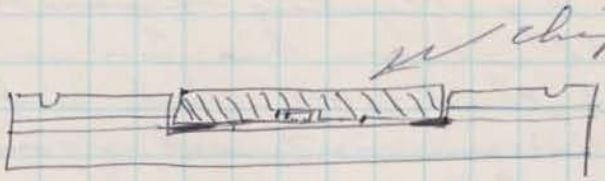
J. K. Killby
July 13, 1958

The detail drawings of the stages with a few slight modifications (Size of transistor tubing, number of holes in etch boards) have been made and are numbered JLK 601-1 thru JLK 601-

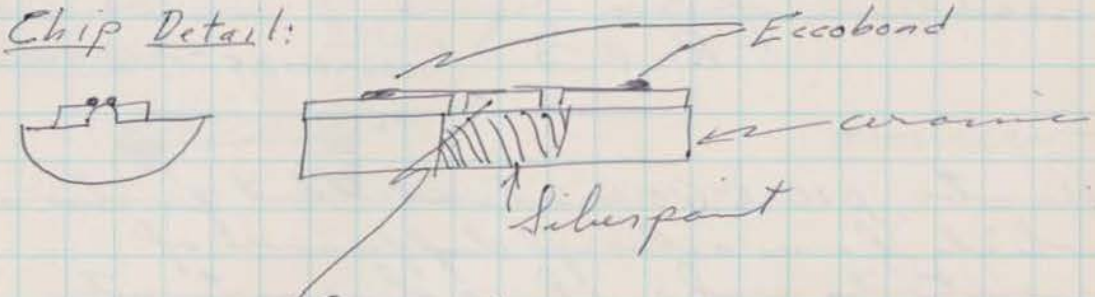
This set of drawings includes details of Grown alloy transistors (-1 + -2), resistors (-3) Tubular capacitors (-4), Plate capacitors (-5), Transformer (-6). Transistor Details,

End plate (-13 + -16), Ten (14) have been completed. Also shown in 601-12 is a Diffused Base transistor structure.

This structure uses a small glass or ceramic chip to support the wafer.



Chip Detail:



J. S. Kilby
July 22, 1958

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EO NO. 043601

DATE July 24, 1958

Extreme miniturization of many electrical circuits could be achieved by making resistors capacitors and transistor & diodes on an angle slice of silicon. If the slice were thin, useful values of resistors could easily be made by attaching ohmic contacts to a small silicon bar. For example, a bar .002 thick, .010 wide, and .100 long, of 1Ω-cm material would have resistance of

$$R = \rho \frac{L}{A} = 1 \frac{.100}{.002 \times .01 \times 2.5} = 2{,}000\ \Omega.$$

Hunter, p10-1 (10.2) shows that junctions which have a large difference of resistivity and a sharp discontinuity of resistivity at the junction have a capacitance

$$C_o = A \left(\frac{K K_o}{2 V \mu \rho}\right)^{1/2}$$

Henry Rice has converted this to a practical system of units:

$$C = 1.36 \times 10^6 A \sqrt{\frac{K}{V \mu \rho}}$$

where A = Junction area in $\square$ in
C = Capacity in μμf
K = Dielectric constant
V = Applied voltage
μ = mobility
ρ = resistivity

For	μ	K
N type Ge	3800	16
P type Ge	1800	16
N type Si	1750	12
P type Si	400	12

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DATE July 29

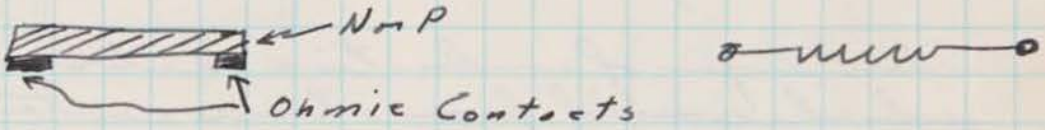
Thus for p type Si which would make the best capacitors,

$$C = 1.36 \times 10^6 \sqrt{\frac{12}{1 \times 400 \times 1}} \approx .25 \mu f/in^2$$

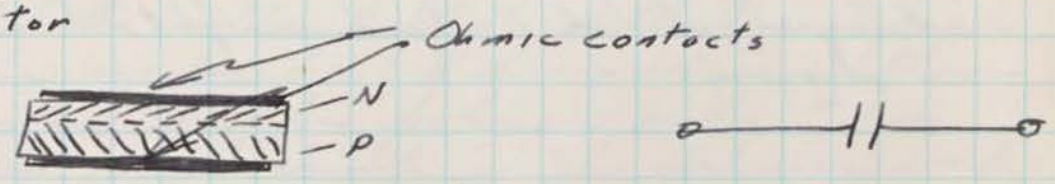
at 1 Volt for 1Ω-cm

The following circuit element could be made on a single slice:

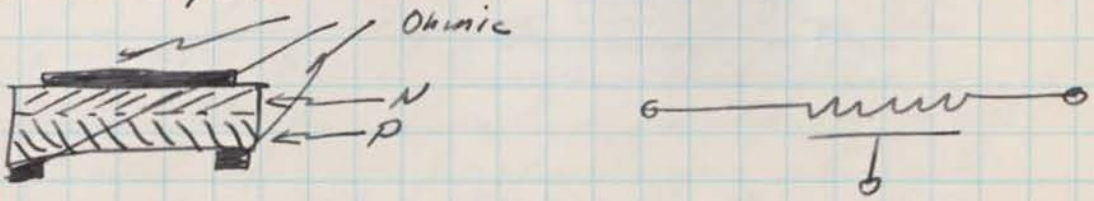
Resistors:



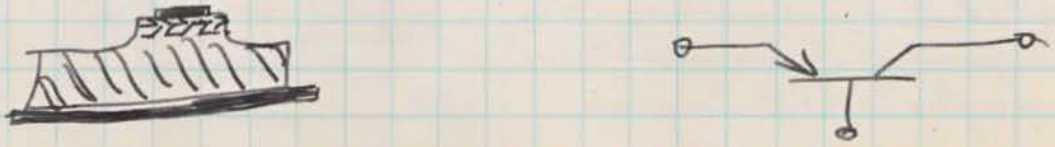
Capacitor



Distributed Capacitor



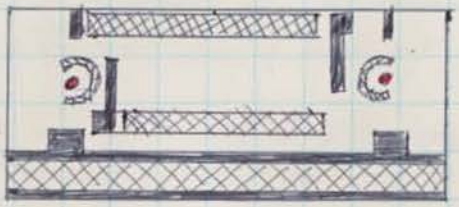
Transistor



A process which might be used for fabricating a circuit on a single crystal slice of Silicon is outlined below.

First, a slice of the proper size would be double diffused - for instance, if a p type wafer is used, a deep n-type skin would be applied, and a shallower p type layer on top of it. Such diffusion is well known, and might be performed in a single step if desired. One side of the wafer would then be lapped off.

Then layers of conductive material which would form ohmic contact with the desired layers of semiconductor would be applied, preferably by evaporation, and alloyed. Such a slice might then look as shown:



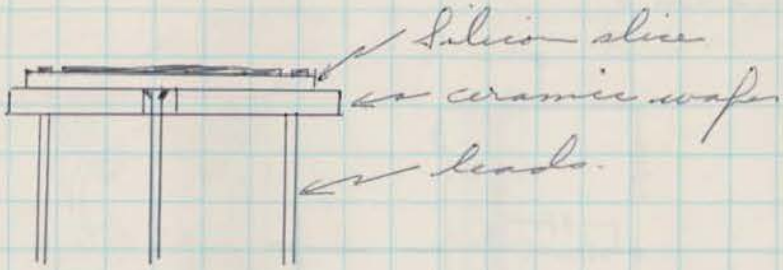
Where

- Material alloyed to contact top n layer
- Material alloyed to contact p layer
- Material alloyed to contact lower n-layer

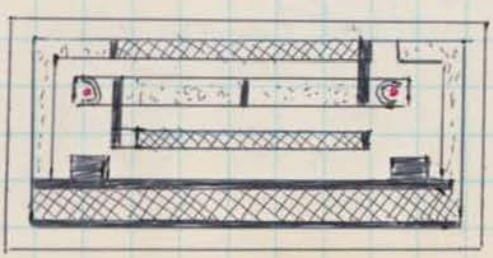
The unit should then be masked and the areas shown in white above would be etched to remove the exposed (and undesired) surface n+p layers.

EO NO. 043601
DATE July 29, 1958

Because the wafer would be extremely thin and fragile at this point, it would be desirable to strengthen it by attaching to an insulating wafer or plate. Such plate probably should be of glass or ceramic.



Leads might also be attached at this time by soldering or welding. They could be attached to either surface of the wafer, but I have shown them attached to the bottom only. This would be desirable if the ceramic wafer was made a part of the seal for the device package, additionally, it keeps the top surface of the wafer free for the processing steps to follow. After attachment to the ceramic blank, the unit could be masked with a photo-resist, and the wafer of silicon etched thru to form the desired circuit



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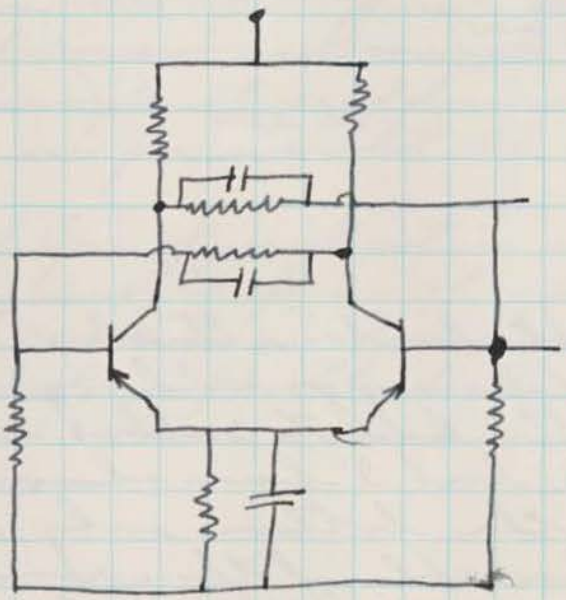
DATE July 24, 1958

This unit might then be machined and conductive material evaporated to connect the transistor emitter + base to the circuit, or small wires might be attached by thermal bonding. In either case, the unit shown would have all of the circuit elements for a multivibrator.



This is the unit used by Apparatus for the intervalometer, and shown on drawing MM-0001

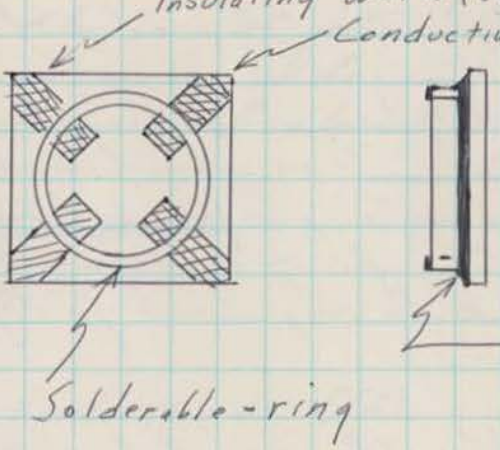
J. S. Kilby

July 24, 1958

EO NO. 043601
DATE August 6, 6

Small Transistor Package

A small, flat transistor package would have use with several types of miniturized schemes, such as DOFL and RCA. Such a package might be constructed in this manner:



The solderable ring might be either a glass or ceramic ring with the top surface metalized, or a metal ring. If a metal ring were used, electrical clearance would be required between the ring and the conductive patterns on the wafer. This could be provided by

1) Using depressions in the wafer for the conductors

2) Using notches in the ring to space it away from the conductors

3) Insulating the metal ring before assembly with a higher temperature enamel.

EO NO. 043601

DATE August 6, 1958

In any case, the structure shown on the preceding page could be made by:

1. Metalizing wafer (screen or plate etch)
2. Dip metal ring in solder glass (2 coats)
3. Put ring in position on plate
4. Heat to about 450°C for 30 minutes
5. Lap off glass on top edge of ring.

A transistor could then be inserted in the cavity & soldered or preferably by Ecobond. The conductor pattern shown would be satisfactory for grown junction unit. Other would be required for diffused base and alloy transistors.

In any case, after the unit has been inserted & tested, a metal cover could be soldered in place to provide a hermetic seal.

These unit could be made extremely small. Sample have been made which are .100 square ± .020 thick. These unit did not use the solder glass, and were not sealed.

J. S. Kilby

August 6, 1958.

EO NO. 3436-01
DATE August 14, 1958

Samples of Silicon R-C combinations have been constructed. A p type chip was diffused on 0.5 Ω cm N type Silicon. One side of the wafer was lapped, and the entire wafer was nickel plated. The wafer was then cut into bars, 0.020 wide, 0.010 thick, and about .400 long. These bars were mounted on headers. The p-type side was marked, and the unit etched. The resulting bar had an end-to-end resistance of about 1000 ohms, and about 160 μμf capacity at 5 Kc.

Bridge Readings as f(f)

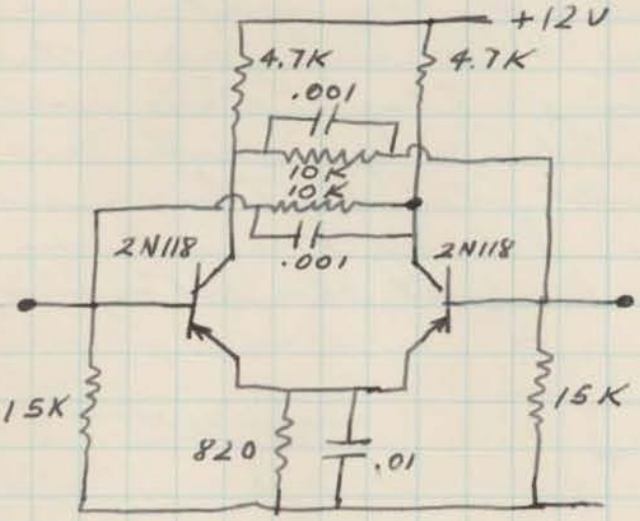
Freq	C	D
2 Kc	250	.79
4 Kc	189	.7
5 Kc	163.5	.675
10 Kc	139.	.75
20 Kc	128.	1.04
40 Kc	103.	1.56

J. S. Kilby
August 14, 1958

EO NO. 043601

DATE August 28, 1958

A multivibrator circuit was selected to show the feasibility of all silicon circuits. The apparatus circuit was used:



Silicon element were prepared for the circuit above. Resistors were made from bars .02 × .01 × .4 and etched to value above ± 20%. Capacitors were made from the same bar size. Capacitors were plated on both sides, and therefore acted as lumped components.

This unit was assembled & tested by feeding square waves thru coupling capacitors into both bases. Unit followed well up to about 20Kc.

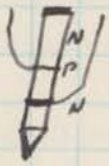
J. S. Kilby

August 28, 1958

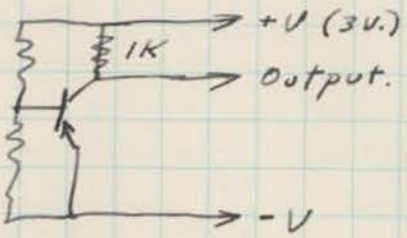
EO NO.

DATE Sept 9, 1958

W.A. adcock has suggested that a grown junction transistor bar might serve as a phonograph.



To test the possibility that this might be useful, I removed the can from a 2N118 Silicon transistor, and connected it in a grounded emitter circuit as shown:



An oscilloscope was connected to the output terminals, and a Burgess Vibratool was used to mechanically excite the unit. About ½ volt output was obtained with the tool tip in contact with the transistor bar near the junction. A second transistor, of the same type was substituted, and only about .1 volts could be obtained. It is believed that the large output of the first unit was due to a poor end connection on one end of the bar. By the end of the test, the first transistor was open under pressure was applied, and it was felt that most of the output was due to this contact resistance.

J.H. Kelley
September 9, 1958

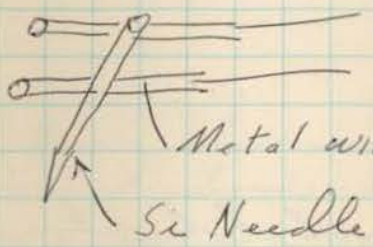
EO NO.

DATE Sept 10, 1958

A phonograph pickup could be built which is dependent upon contact resistance between two semiconductor ~~pb~~ blocks, or between one block and metal contact. One form which might be used:

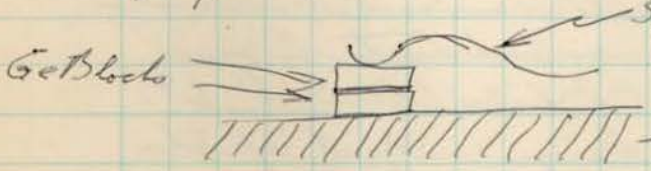
Plating could be provided on the back of each wafer, and a needle or chuck soldered to one side. Unit would have to be preloaded by a spring or resilient plastic case.

Another version which might be useful:



This would use a silicon needle pressed against two wires. Variation in contact pressure would occur with deflection of the needle. Again, preloading of ~~two~~ pressure would probably be desirable.

I have used two flat, lapped germanium wafers, placed together in a capacitance test jig as shown.



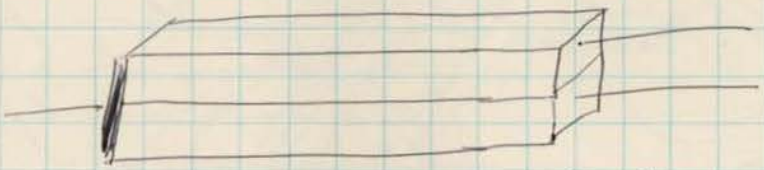
When excited with a Vibratool, about 0.2 volt pp was available with the point about an inch away from the blocks.

J. Kilby
September 10, 1958

EO NO.

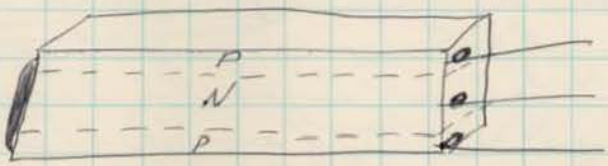
DATE Sept 10, 1968

A phonograph pickup could also be made using the piezoelectric effect of germanium. A bimorph structure would probably provide the greatest output. This structure could easily be made using a diffusion process as shown:



Conventional Bimorph Structure

The proposed structure would be:

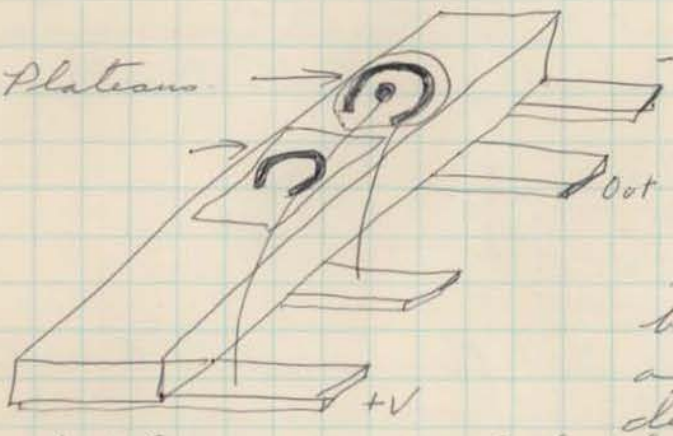


The resistivity of the center section could be low enough so that all connections could be made at one end. The needle could be soldered to the other end, or a one piece version could be used:

In this case the end of the bar would be pointed to serve as a needle.

J. S. Kilby
September 10, 1968

A wafer of germanium has been prepared as shown to form a phase shift oscillator.



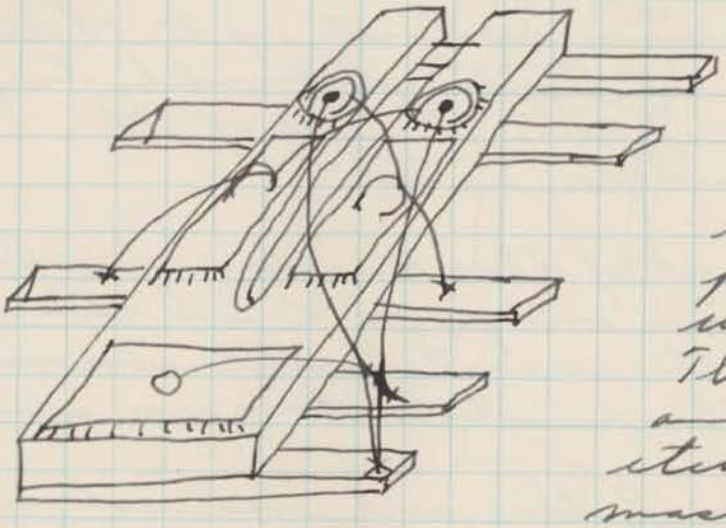
The bulk resistance of the germanium was used for resistor, and a p-n junction for a capacitor. The p type Ge wafer was diffused by conventional technique, and an aluminum emitter dot was evaporated & alloyed. Gold was evaporated and alloyed to provide connection to the transistor base and to the capacitor area. Plateaus were formed by etching for the transistor and capacitor. Tabs were attached to make contact with the Germanium wafer as shown. ~~Gold~~ The wafer was mounted on a glass slide with Sauereisen cement, and gold wires bonded thermally to make the necessary interconnections. The unit was then given a clearcoat.

When 10 volts were applied (1000 Ω series current limiting resistor), the unit oscillated at about 1.3 Mc, amplitude about 0.2 v pp. This test was witnessed by W.A. Alcock, Bob Pritchard, Mark Shepard, and others.

J.S. Kilby
September 12, 1958

EO NO. 043601
DATE Sept 19, 1958

In order to further test the feasibility of circuits on a single crystal wafer, I have had three units made up as shown:



These units were made from diffused material which had been prepared for developmental work on the 2N623. The wafers were lapped and the slot was etched using a wax mask. Gold plated platinum tabs were alloyed to the back of the wafers. The emitter + base contacts, including those which serve as contacts for the capacitors, were evaporated on before the slot was etched. Platforms for the transistor and capacitor areas were masked, using wax, and etched. The bar was then cemented to a piece of microscope slide using Sauereisen Cement. Gold wire was thermocoupled to the contact areas, and the other ends of the wire Ecobonded to the gold tabs. These units were fabricated by Tom Yeargen from my sketch.

On testing, it was found that one unit, using a 7 volt supply, would act as a bi-stable device. That is, by grounding the base lead alternately,

first one transistor would conduct & then the other. With an AC signal applied, the unit acted more as a monostable MV. It did exhibit good square wave output up to 150 Kc, and seemed to be definitely triggering up to 600 Kc, the limit of the signal generator used.

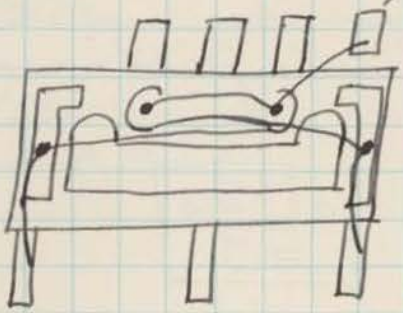
The circuit of this device is identical to that shown on page 12, — this unit has all of the circuit elements shown there, although the resistor values are smaller.

Operation of this unit was witnessed by W. A. Adcock, Mark Shepard, and others.

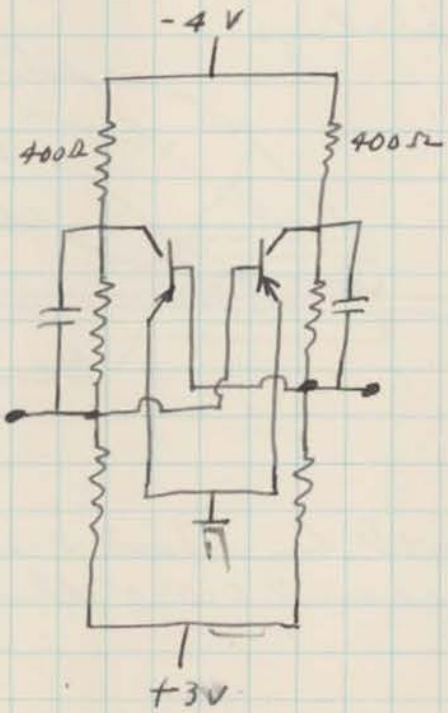
J. S. Kilby
September 19, 1958

EO NO. 043607
DATE October 1, 195

I have completed a set of sketches showing a much smaller version of a similar MV. This unit will have a wafer shaped as shown:



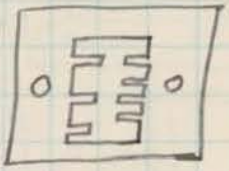
The circuit is



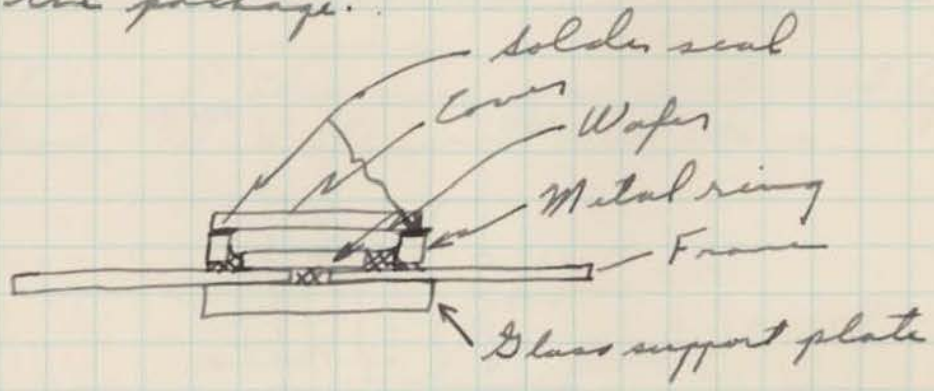
This circuit was developed by Jerry Tucker as a saturated flip flop for a 2 Mc rep rate using 2N623's.

These sketches also illustrate another feature, which I have not used before on these units. This is a method of making

all of the leads from a single piece of material, as by blanking. This part, or frame, will be provided with pilot holes which can be used to locate the unit in all subsequent assembly steps.



I have also provided a method of hermetically sealing the package.



This unit should be about 0.240" long, 0.120" wide, and will not exceed 0.030" thick. 10 components are included.

The process for producing these units, or others of similar type, might be:

1. Polish wafer
2. Diffuse
3. Cut to size
4. Lap to 0.003
5. Alloy to leads
6. Element wafer + leads to support using solder glass

EO NO. 043601

DATE Oct 1, 1958

7. Etch slot after masking with photoresist
8. Evaporate & alloy base & emitter
9. Plate mask transistor & capacitor pads
10. Gold bond wires
11. Clean up etch
12. Solder cover
13. Final test.

J. S. Kilby
October 1, 1958

EO NO. 043601

DATE October 21, 1958

The mechanization model shop has completed a model of the MV design shown on p 23. This unit is 10X actual size.

J.D. Kelly
October 21, 1958

EO NO. 043601

DATE October 29, 195

I have shown the sketches mentioned on p 23 to Bob Frank. He will order tooling.

It would appear that we may have some difficulty designing a circuit to work over a wide temperature range using the ~~to~~ 2 Ω cm material now used in the collector region. I will check on the possibility of using the diffused emitter + base layers as resistors. If serious impurity scattering is present, or if the layers are thin enough, they may have a temperature coefficient similar to metals - or at least better than what we now have to cope with.

J. A. Kilby

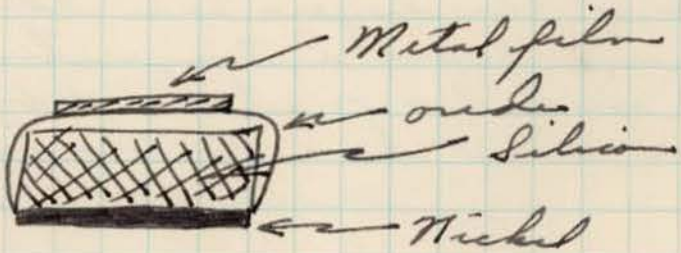
28

EO NO. 043604

DATE November 24, 1958

I have obtained some silicon wafers from Jay Lathrop which were polished and oxidized at 1200°C. Two of these were made into capacitors by evaporating a metal contact over the oxide layer. Aluminum was used for the first unit, and gold for the second.

An ohmic contact was made to the Silicon by lapping + plating with electroless nickel.



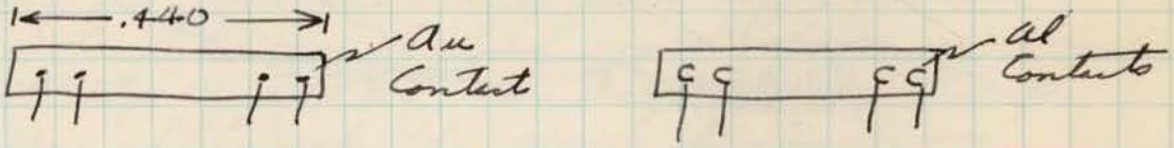
Lathrop estimated the film thickness as 7300 Angstroms from interference measurements. Measured capacitance on the two parts was about 2100 μμf, ±1% as measured on GR 1611-B Bridge. This bridge applies about 50 volts of 60 ~ AC to samples of this type.

Lathrop etched a third unit oxide layer down to about 5500 A. This unit was shorted on initial test. When the unit was broken in two, one half (approx.) was checked + permitted readings. Oxide layer thickness can apparently be calculated fairly well by using K = 3.8.

J. H. Kelley

EO NO. 043604
DATE Dec 2, 1958

To test the feasibility of using the diffused layers as resistors, I have obtained a wafer from diffusion run GP-23 from Dal Little. These were evaporated with aluminum and with gold per usual production practice, and alloyed. The wafer was then cut into bars, and leads were bonded.



Emitter Layer Test Bar Base Layer Test Bar

Contacts were checked for rectification with an ohmmeter. No significant change was found on reversing leads, or changing scales.

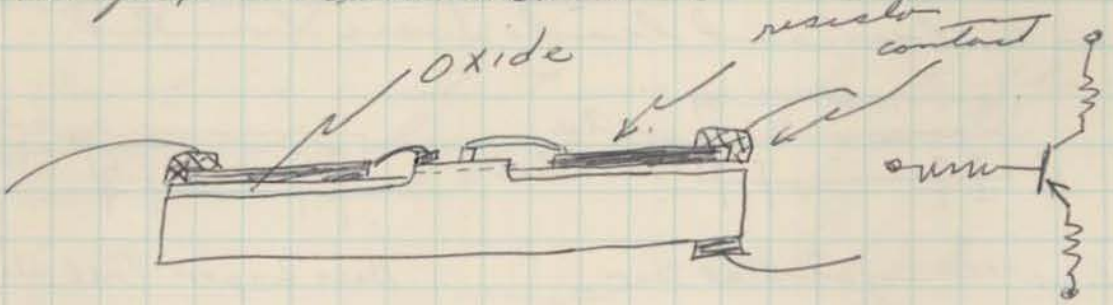
Base Layer #1		Emitter Layer #2	
27°C	11 K	27°C	12.4K
50°C	11 K	100°C	11.7K
67°C	11 K	123°C	11.6 K
75°C	10.9K	27°C	12.5 K
90°C	10.95K		
100°C	10.9 K		
125°C	10.9K		
28°C	11.1 K		

These tests must be rerun with a more accurate resistance measuring device, but the stability with temperature is excellent — much better than expected from data on bulk material which I have seen.

J. A. Kilby
December 2, 1958

30
EO NO. 043604
DATE Dec 3, 1958

Another way in which more stable resistors might be formed would be by evaporation of a resistance material such as nichrome onto a semiconductor substrate. If desired, an oxide layer could be used as silicon to provide insulation.



This might be used in conjunction with base layer resistors, as shown above, or with emitter layer resistors.

Additionally, capacitors might be formed ~~on~~ by using the capacitance between the resistor and the substrate, or by ~~a~~ evaporation of a dielectric layer over a conductive area and evaporation of a second conductive layer over the dielectric layer. Complete circuits could be fabricated in this manner.

This scheme was discussed with WA Adcock on a trip to Washington, DC on August 5, 1958, but has not been previously recorded.

J L Kilby
December 3, 1958

EO NO. 0043604

DATE Jan 9, 1959

I have completed two samples of the multivibrator described on page 23 of this note book. On test, it was necessary to apply 6 or 7 volts rather than the design value of 4 volts before the unit would switch. It is believed that this is probably due to low beta transistors. The beta falls off badly on transistors of this type at low currents. The unit had good ~~wave~~ wave forms up to 200 Kc, and followed up to 1 Mc, although the wave form was badly rounded.

J S Killy

9 January 1959

32
EO NO. 0043604
DATE Feb 7, 1959

I have completed a series of four layouts for circuit submitted for ARMA. These circuits are

1. Diode "And" Gate — Arma A13
2. Multivibrator Input Gate — Arma A21
3. Multivibrator Half — Arma SF1
4. Inverter — Arma CB1/CB2

The original Arma layout showed a 2 input gate + a 3 input gate. The 3 input gate can be used for both applications

The original Arma circuit also showed 2 inverter types, differing only in their input arrangements. These have been combined into a single package, CB-1 + CB-2.